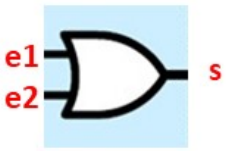
FUNDAMENTOS DE COMPUTADORES I

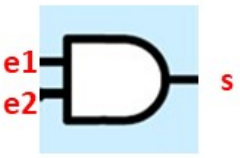
CUADERNO DE LA PRÁCTICA 2

Componentes del sumador de un bit

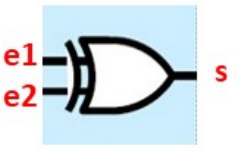
```
ENTITY or2 IS
  PORT( e1, e2 : IN bit; s : OUT bit);
END or2;

ARCHITECTURE comportamiento OF or2 IS
BEGIN
  s <= e1 OR e2;
END comportamiento;
```




```
ENTITY and2 IS
  PORT(e1, e2 : IN bit; s : OUT bit);
END and2;

ARCHITECTURE comportamiento OF and2 IS
BEGIN
  s <= e1 AND e2;
END comportamiento;
```

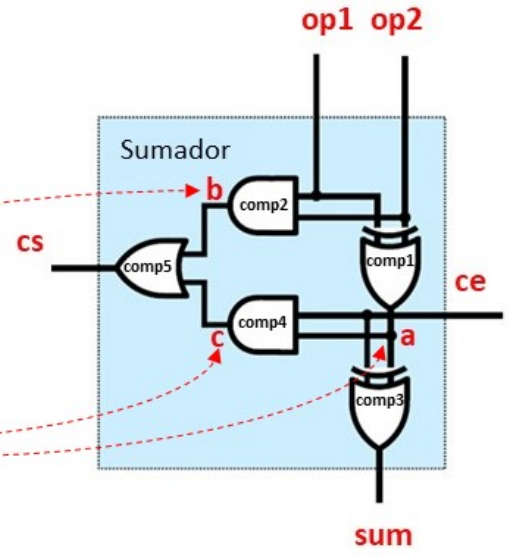



```
ENTITY xor2 IS
  PORT(e1, e2 : IN bit; s : OUT bit);
END xor2;

ARCHITECTURE comportamiento OF xor2 IS
BEGIN
  s <= e1 XOR e2;
END comportamiento;
```



Sumador de un bit

```
ENTITY sumador IS
  PORT(op1, op2, ce : IN bit;  sum, cs : OUT bit);
END sumador;

ARCHITECTURE puertas OF sumador IS

-- Declaracion de componentes
  COMPONENT or2
    PORT(e1, e2 : IN bit; s : OUT bit);
  END COMPONENT;
  COMPONENT and2
    PORT(e1, e2 : IN bit; s : OUT bit);
  END COMPONENT;
  COMPONENT xor2
    PORT(e1, e2 : IN bit; s : OUT bit);
  END COMPONENT;

-- Declaración de señales de interconexion
  SIGNAL a, b, c : bit;

-- Interconexion de componentes
BEGIN
  comp1 : xor2  PORT MAP(op1, op2, a);
  comp2 : and2  PORT MAP(op1, op2, b);
  comp3 : xor2  PORT MAP(a, ce, sum);
  comp4 : and2  PORT MAP(a, ce, c);
  comp5 : or2  PORT MAP(b, c, cs);

END puertas;
```



Esquema de interconexión del sumador de 2 bits

Código VHDL del sumador de 2 bits