

Device Operation & Timing Diagram

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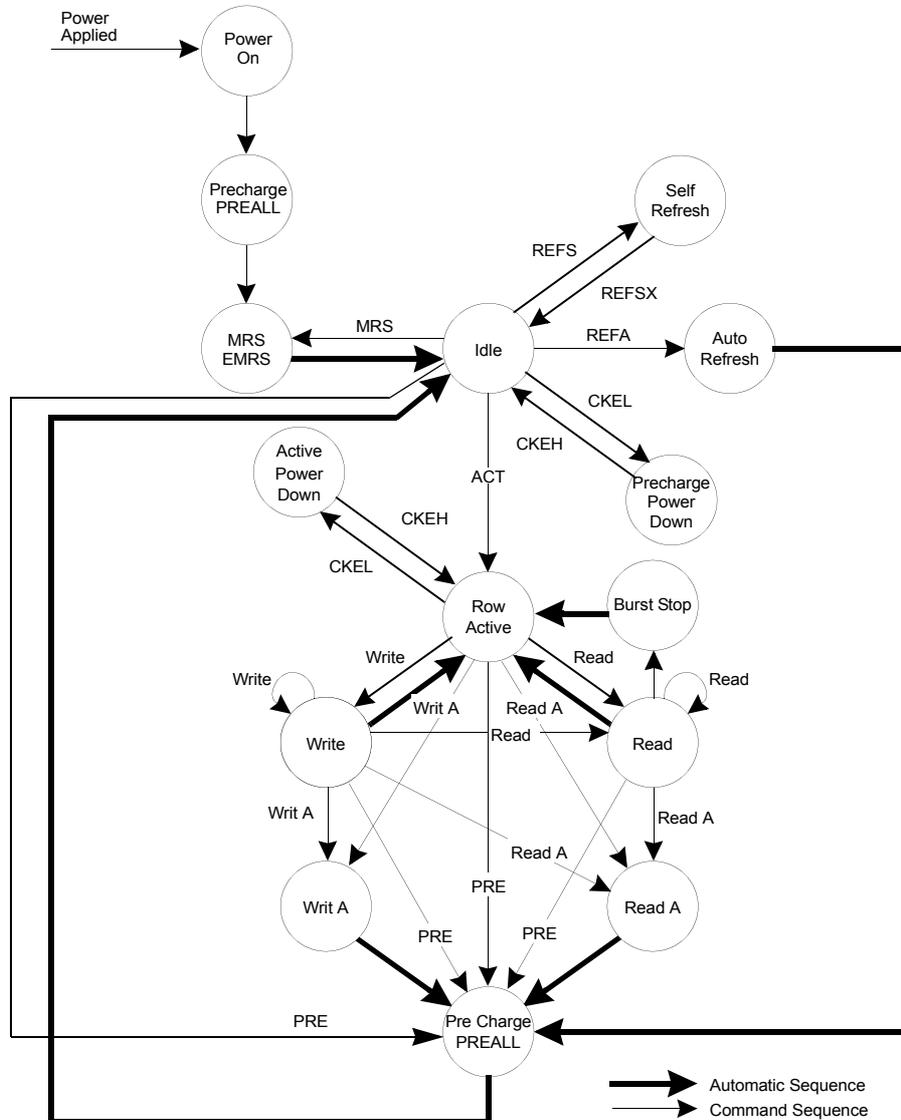
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Device Operation

Simplified State Diagram



Power-up & Initialization Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. No power sequencing is specified during power up and power down given the following

- V_{DD} and V_{DDQ} are driven from a single power converter output, AND
- V_{TT} is limited to 1.35 V, AND
- V_{REF} tracks $V_{DDQ}/2$ OR, the following relationships must be followed:
- V_{DDQ} is driven after or with V_{DD} such that
- $V_{DDQ} < V_{DD} + 0.3$ V AND
- V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3$ V, AND
- V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3$ V.

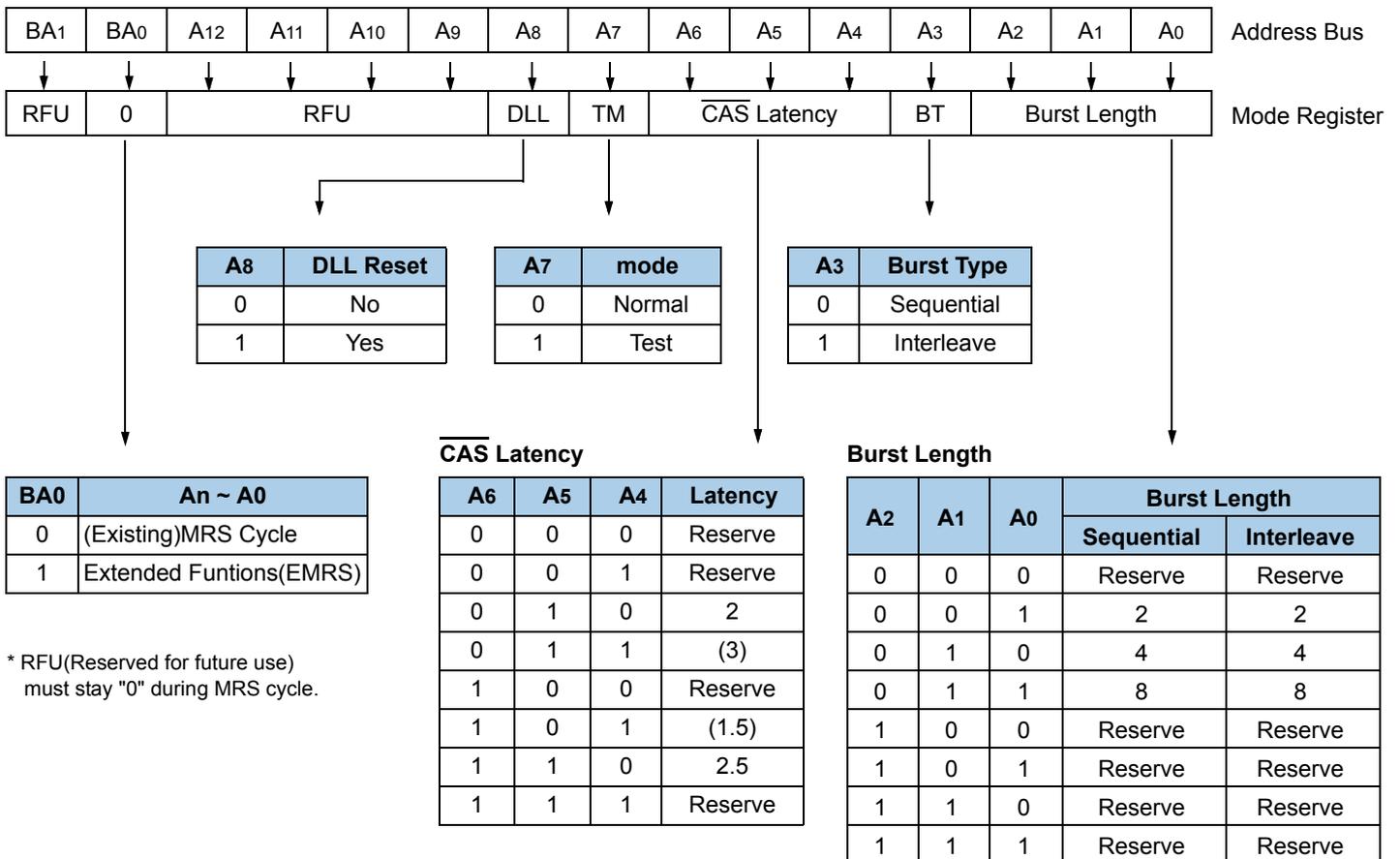
At least one of these two conditions must be met.

Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V_{DD} is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μ s delay prior to applying an executable command. Once the 200 μ s delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRE-CHARGE ALL command should be applied, placing the device in the "all banks idle" state. Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

Mode Register Definition

Mode Register Set(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{\text{CAS}}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0(The DDR SDRAM should be in all bank precharge with $\overline{\text{CKE}}$ already high prior to writing into the mode register). The states of address pins A0 ~ A11(*1A12) in the same cycle as $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 going low are written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, $\overline{\text{CAS}}$ latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst lengths, addressing modes and $\overline{\text{CAS}}$ latencies.

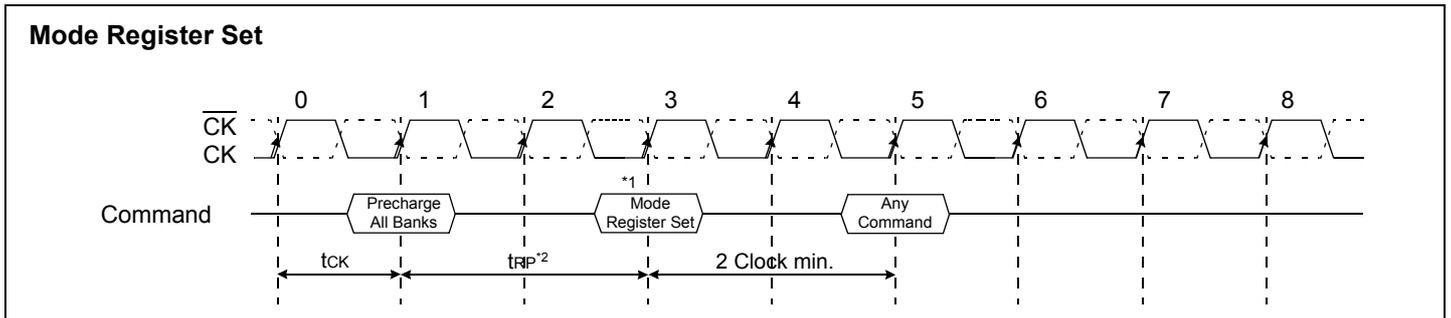


* RFU(Reserved for future use) must stay "0" during MRS cycle.

Note : *1 A12 is used for 256Mb only. That is 128Mb uses A0~A11, 256Mb A0~A12.

Burst Address Ordering for Burst Length

Burst Length	Starting Address(A2, A1, A0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

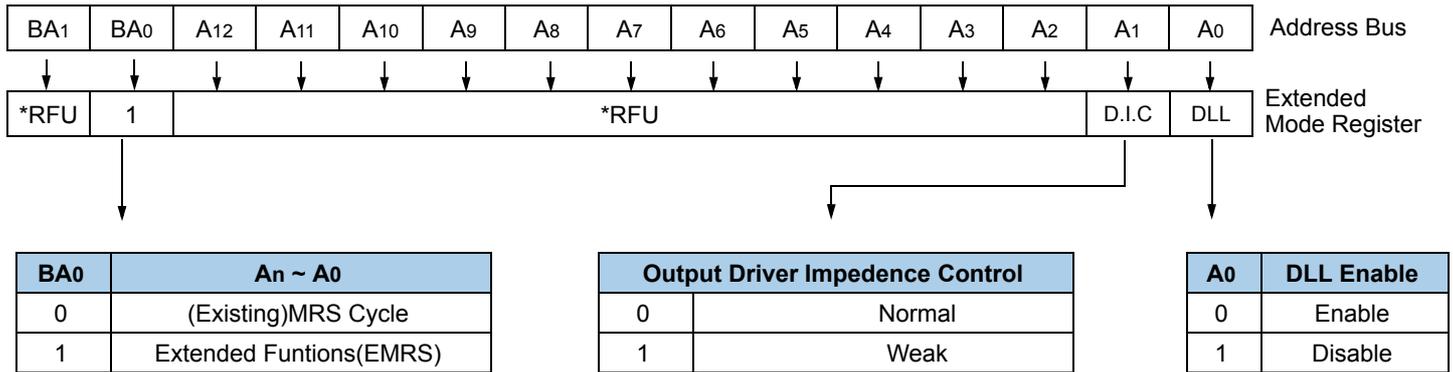


*1 : MRS can be issued only at all bank precharge state.

*2 : Minimum tRP is required to issue MRS command.

Extended Mode Register Set(EMRS)

The extended mode register stores the data for enabling or disabling DLL, and selecting output driver size. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11(¹A12) and BA1 in the same cycle as \overline{CS} , \overline{RAS} , \overline{CAS} and \overline{WE} going low are written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



*RFU : Must be set "0"

Figure 7. Extend Mode Register set

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Samsung supports a weak driver strength option, intended for lighter load and/or point-to-point environments. I-V curves for the normal drive strength and weak drive strength are included in 11.1~2 of this document.

Precharge

The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when \overline{CS} , \overline{RAS} and \overline{WE} are low and \overline{CAS} is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses(BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied until the precharge command can be issued. After tRP from the precharge, an active command to the same bank can be initiated.

Bank Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

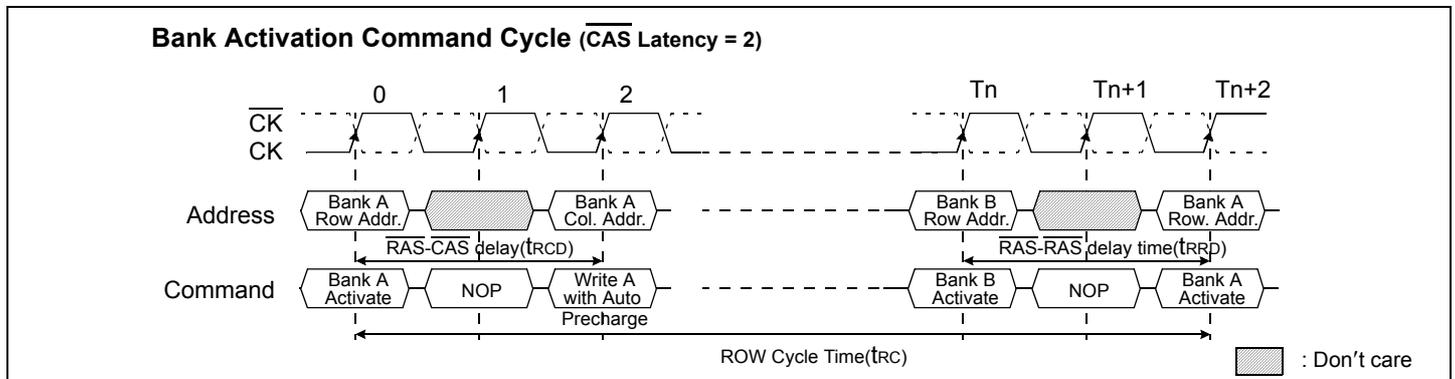
No Operation(NOP) & Device Deselect

The device should be deselected by deactivating the \overline{CS} signal. In this mode DDR SDRAM should ignore all the control inputs. The DDR SDRAMs are put in NOP mode when \overline{CS} is active and by deactivating \overline{RAS} , \overline{CAS} and \overline{WE} . For both Deselect and NOP the device should finish the current operation when this command is issued.

Row Active

The Bank Activation command is issued by holding \overline{CAS} and \overline{WE} high with \overline{CS} and \overline{RAS} low at the rising edge of the clock(CK). The DDR SDRAM has four independent banks, so two Bank Select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of \overline{RAS} to \overline{CAS} delay time(t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(t_{RRD} min).

Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.



Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating \overline{RAS} , \overline{CS} , \overline{CAS} , and deasserting \overline{WE} at the same clock sampling(rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

Write Bank

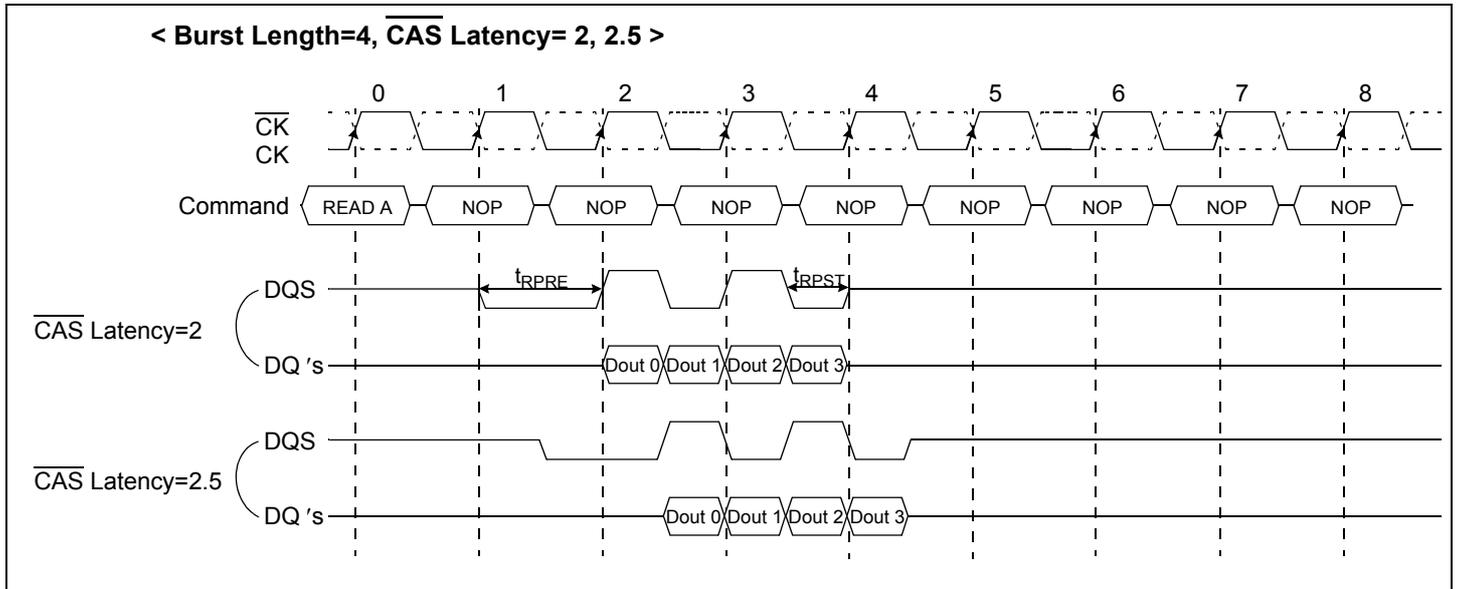
This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating \overline{RAS} , \overline{CS} , \overline{CAS} , and \overline{WE} at the same clock sampling(rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Essential Functionality for DDR SDRAM

The essential functionality that is required for the DDR SDRAM device is described in this chapter

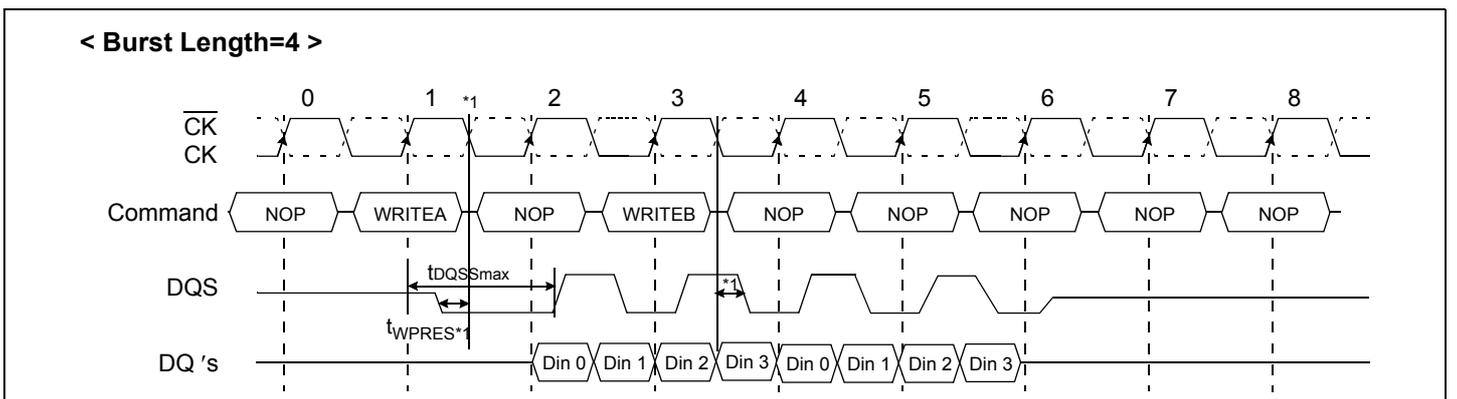
Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting \overline{CS} and \overline{CAS} low while holding \overline{RAS} and \overline{WE} high at the rising edge of the clock(CK) after tRCD from the bank activation. The address inputs (A0~A9) determine the starting address for the Burst. The Mode Register sets type of burst(Sequential or interleave) and burst length(2, 4, 8). The first output data is available after the \overline{CAS} Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe(DQS) adopted by DDR SDRAM until the burst length is completed.



Burst Write Operation

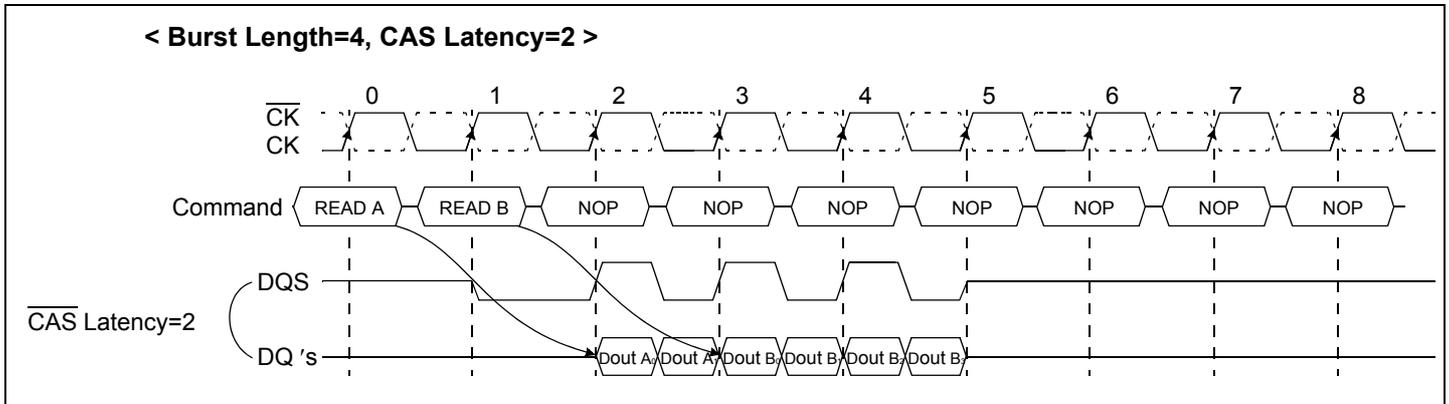
The Burst Write command is issued by having \overline{CS} , \overline{CAS} , and \overline{WE} low while holding \overline{RAS} high at the rising edge of the clock(CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins t_{DS}(Data-in setup time) prior to data strobe edge enabled after t_{DQSS} from the rising edge of the clock(CK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.



* 1. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.

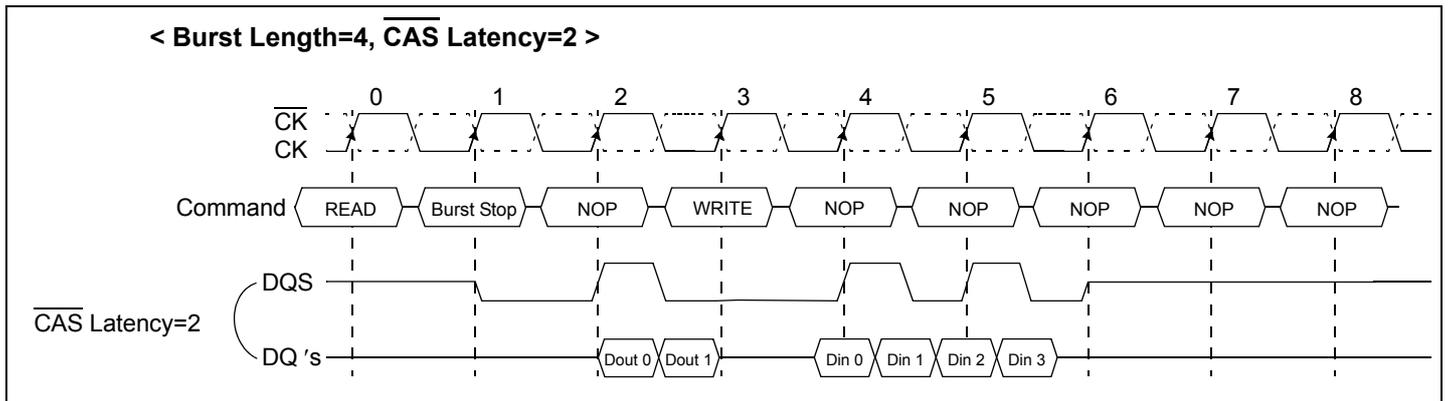
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.



Read Interrupted by a Write & Burst Stop

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's (Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burst stop command must be applied at least 2 clock cycles for CL=2 and at least 3 clock cycles for CL=2.5 before the Write command.

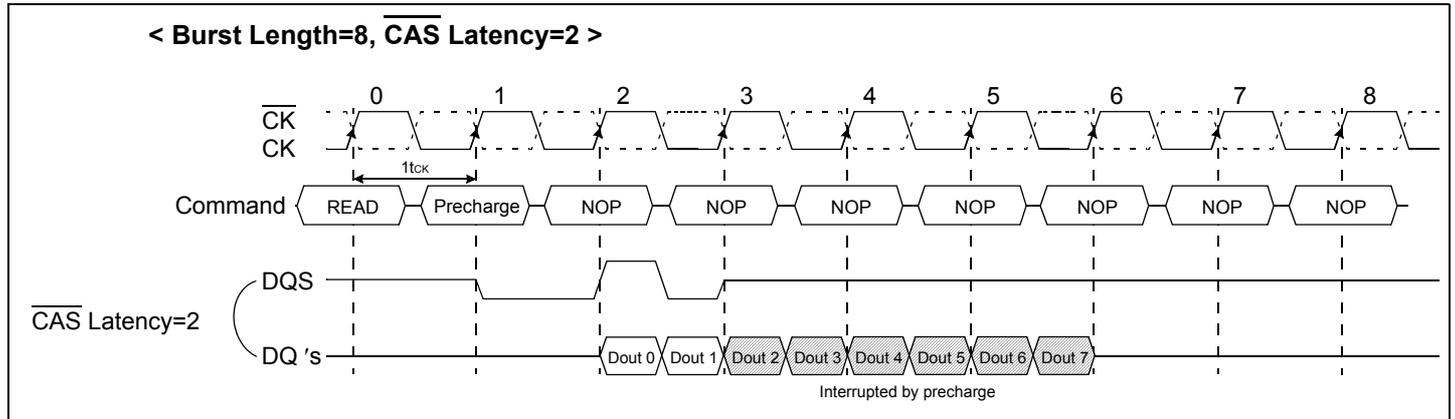


The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = $RU(CL)$ [CL is the CAS Latency and RU means round up to the nearest integer.
2. It is illegal for a Write command to interrupt a Read with autprecharge command.

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the $\overline{\text{CAS}}$ latency.



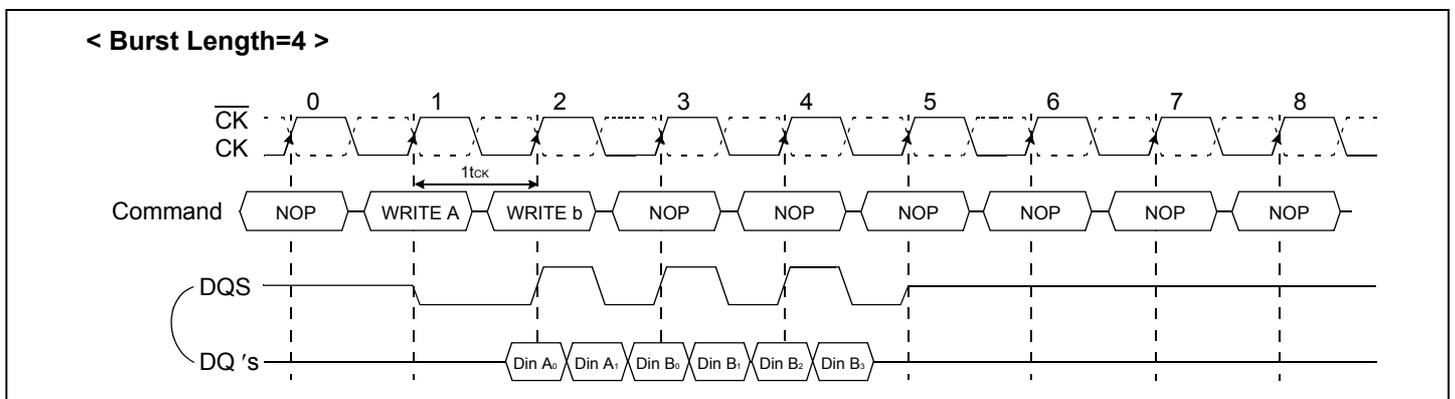
When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{\text{CAS}}$ Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{\text{CAS}}$ Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.
3. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP where tRP begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{\text{CAS}}$ Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.
4. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a rising clock edge).

In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

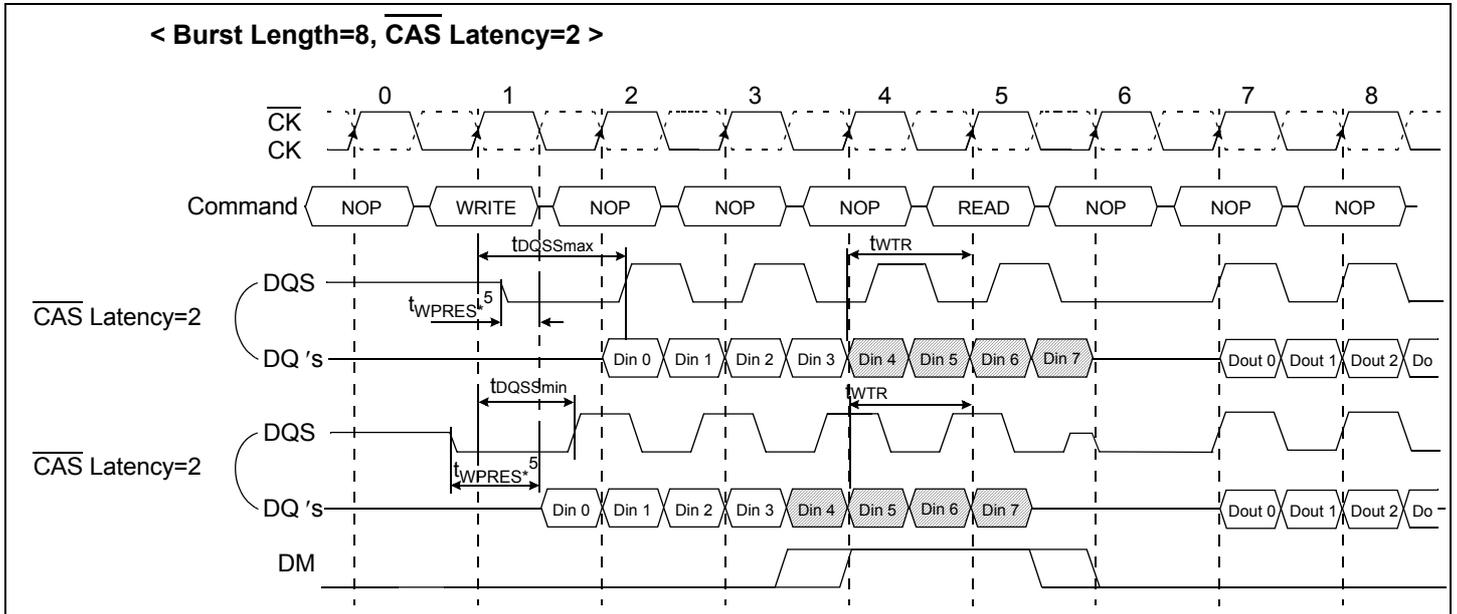
Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.



Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{CDLR}) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

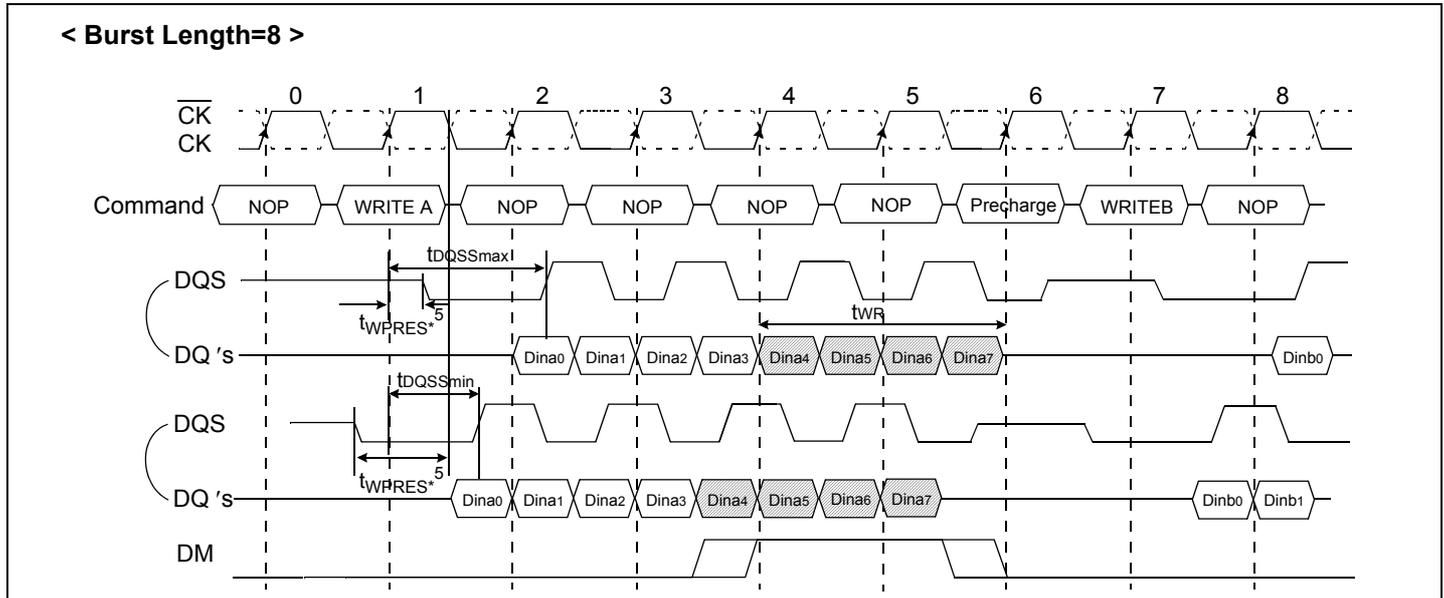


The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the DDR SDRAM.
5. Refer to "3.3.2 Burst write operation"

Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time (t_{WR}) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



Precharge timing for Write operations in DRAMs requires enough time to allow "write recovery" which is the time required by a DRAM core to properly store a full "0" or "1" level before a Precharge operation. For DDR SDRAM, a timing parameter, t_{WR} , is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

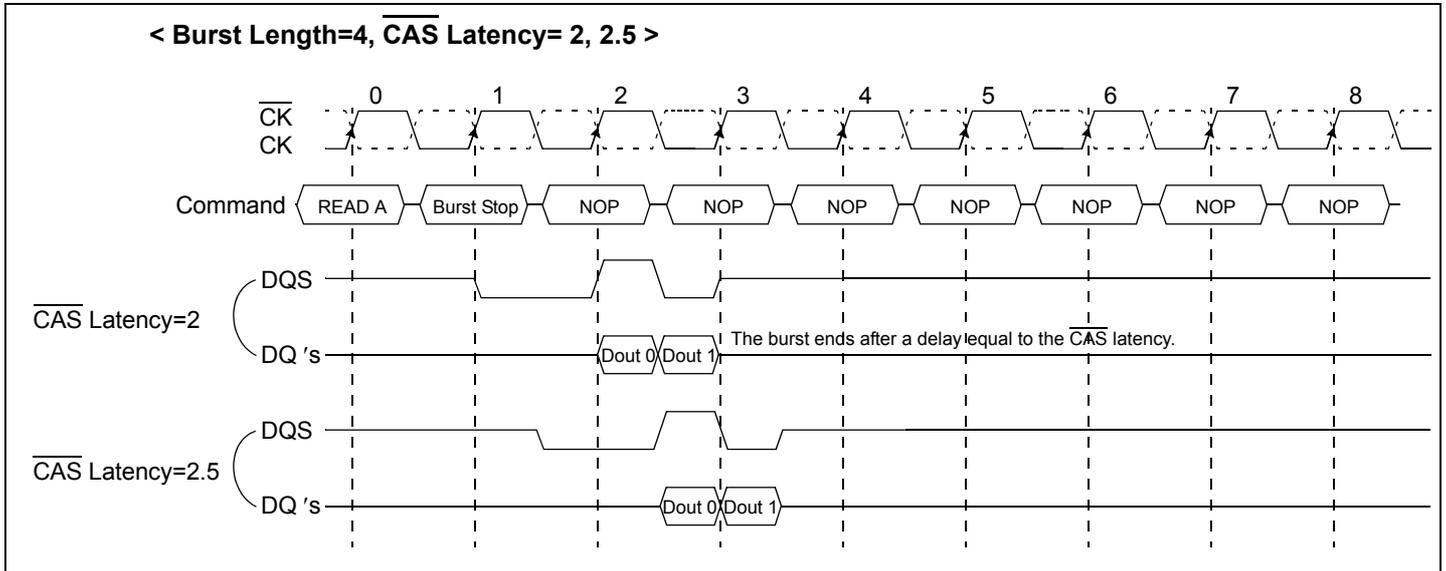
The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the SDRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation, i.e., the input clock domain.

t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR} .
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by t_{WR} .
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after $t_{WR}+t_{RP}$ where $t_{WR}+t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless $t_{RAS(min)}$ [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where $t_{RAS(min)}$ must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.
5. Refer to "3.3.2 Burst write operation"

Burst Stop

The burst stop command is initiated by having $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high with $\overline{\text{CS}}$ and $\overline{\text{WE}}$ low at the rising edge of the clock (CK). The burst stop command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. The burst stop command, however, is not supported during a write burst operation.



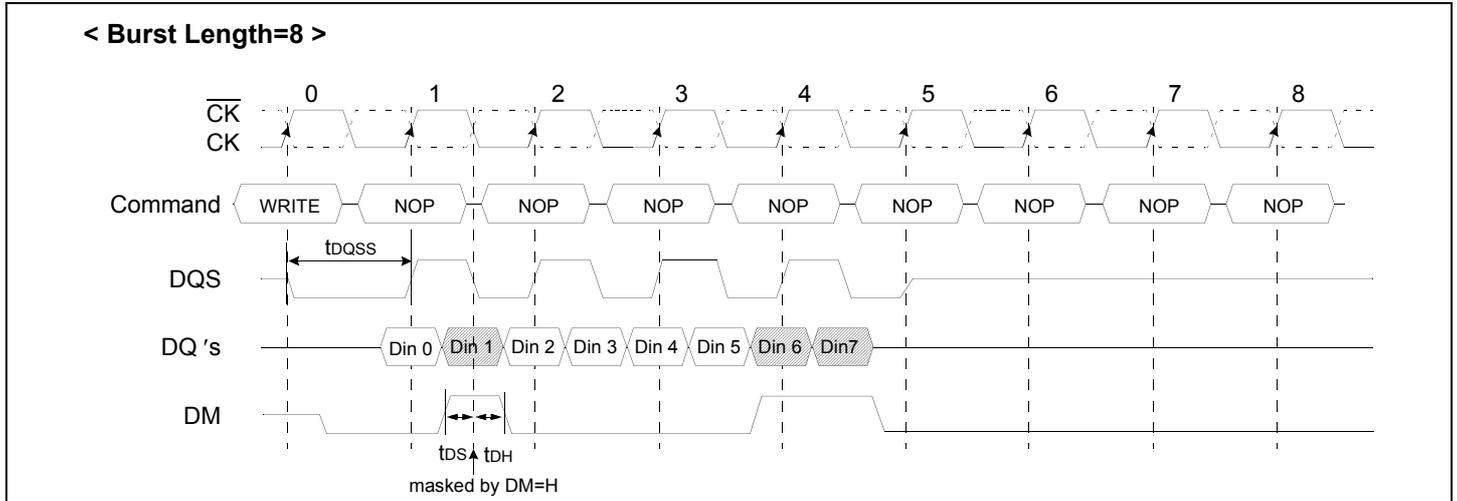
The Burst Stop command is a mandatory feature for DDR SDRAMs. The following functionality is required:

1. The BST command may only be issued on the rising edge of the input clock, CK.
2. BST is only a valid command during Read bursts.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{\text{CAS}}$ latency for read operations. This is shown in previous page Figure with examples for $\overline{\text{CAS}}$ latency (CL) of 1.5, 2, 2.5, 3 and 3.5 (only selected $\overline{\text{CAS}}$ latencies are required by the DDR SDRAM standards, the others are optional).
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).

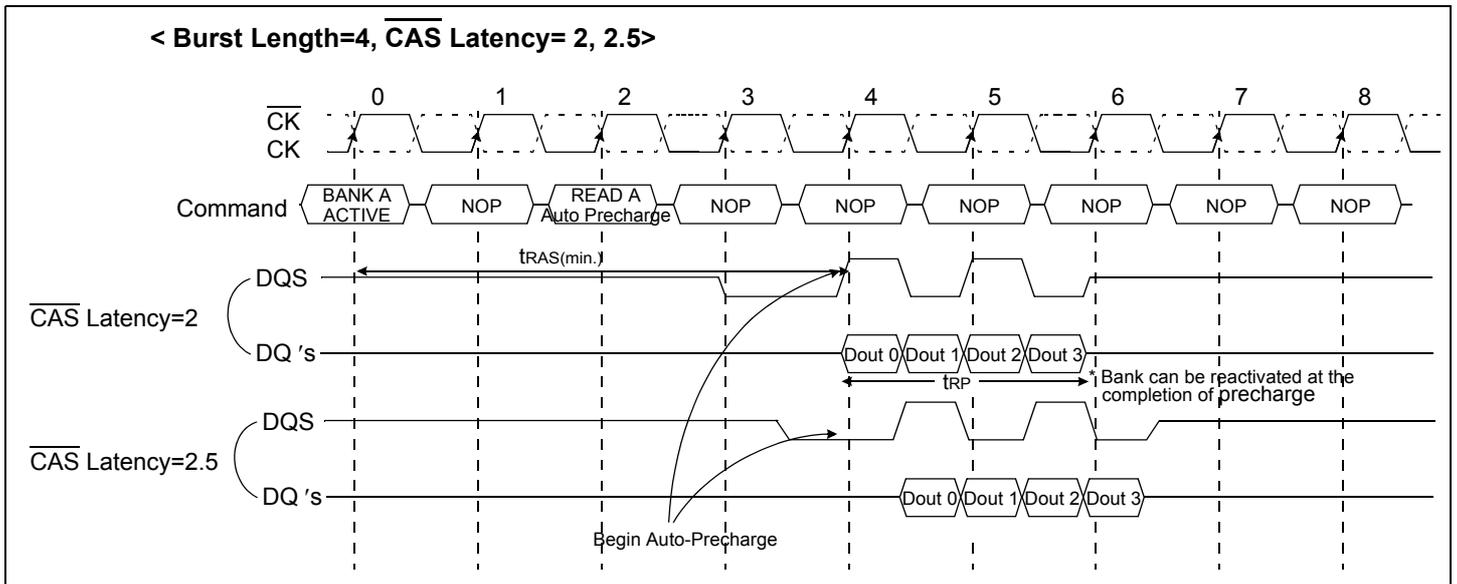
DM masking

The DDR SDRAM has a data mask function that can be used in conjunction with data write cycle, not read cycle. When the data mask is activated (DM high) during write operation, DDR SDRAM does not accept the corresponding data. (DM to data-mask latency is zero). DM must be issued at the rising or falling edge of data strobe.



Read With Auto Precharge

If a read with auto-precharge command is initiated, the DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when $t_{RAS}(min)$ is satisfied. If not, the start point of precharge operation will be delayed until $t_{RAS}(min)$ is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time (t_{RP}) has been satisfied.



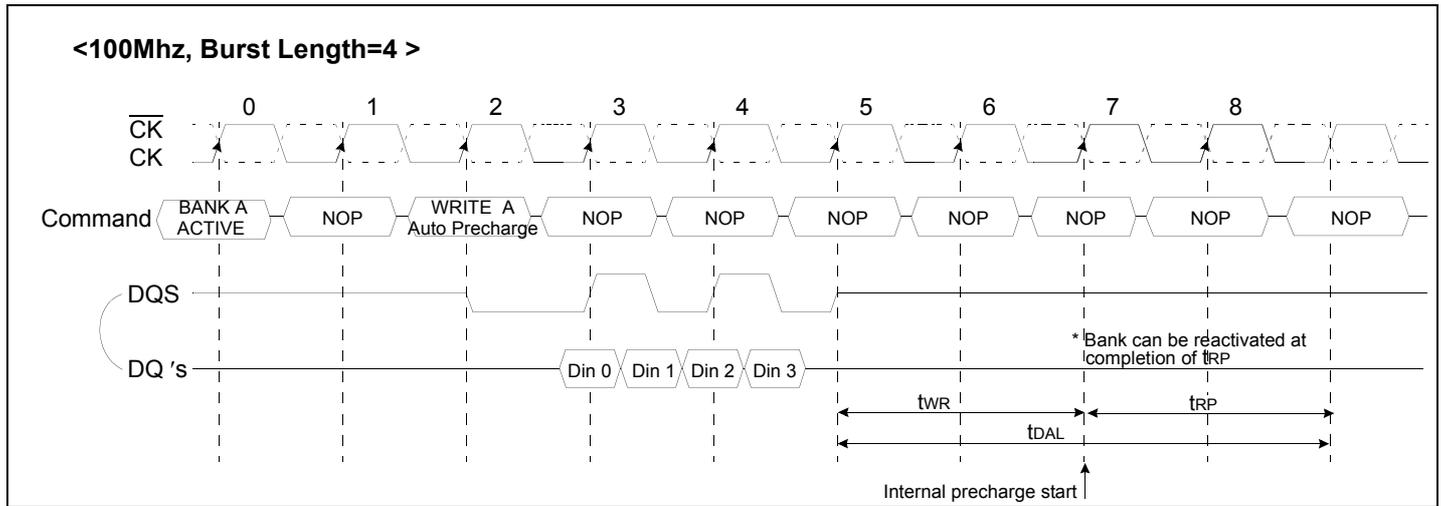
When the Read with Auto precharge command is issued, new command can be asserted at 3,4 and 5 respectively as follows.

Asserted command	For same Bank			For Different Bank		
	3	4	5	3	4	5
READ	READ +No AP ^{*1}	READ+No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

*1 : AP = Auto Precharge

Write with Auto Precharge

If A10 is high when write command is issued, the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping $t_{WR}(\min)$.



Burst length = 4

Asserted command	For same Bank						For Different Bank				
	3	4	5	6	7	8	3	4	5	6	7
WRITE	WRITE+ No AP ^{*1}	WRITE+ No AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE+ AP	WRITE+ AP	WRITE+ AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ+NO AP+DM ^{*2}	READ+NO AP+DM	READ+NO AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ+AP	Illegal	READ + AP+DM	READ + AP+DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

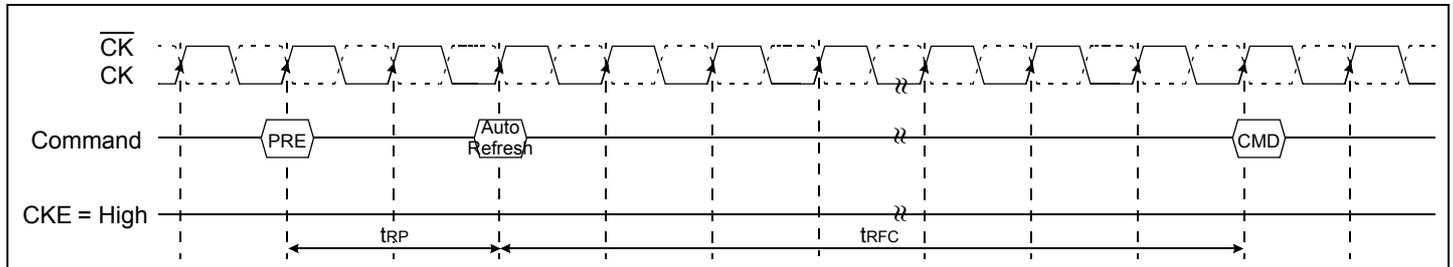
*1 : AP = Auto Precharge

*2 : DM : Refer to " 3.3.7 Write Interrupted by a Read & DM " in page 25.

Auto Refresh & Self Refresh

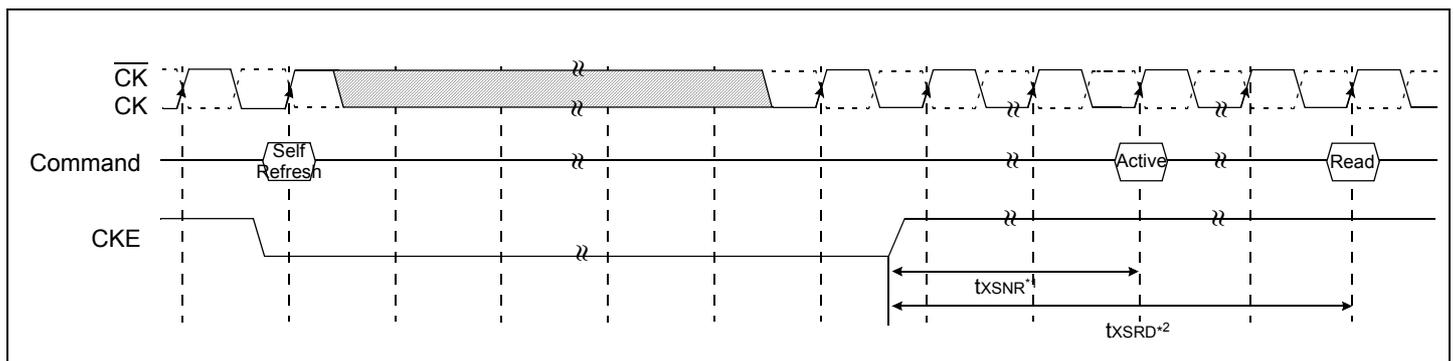
Auto Refresh

An auto refresh command is issued by having \overline{CS} , \overline{RAS} and \overline{CAS} held low with \overline{CKE} and \overline{WE} high at the rising edge of the clock(CK). All banks must be precharged and idle for $t_{RP}(\text{min})$ before the auto refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the $t_{RFC}(\text{min})$.



Self Refresh

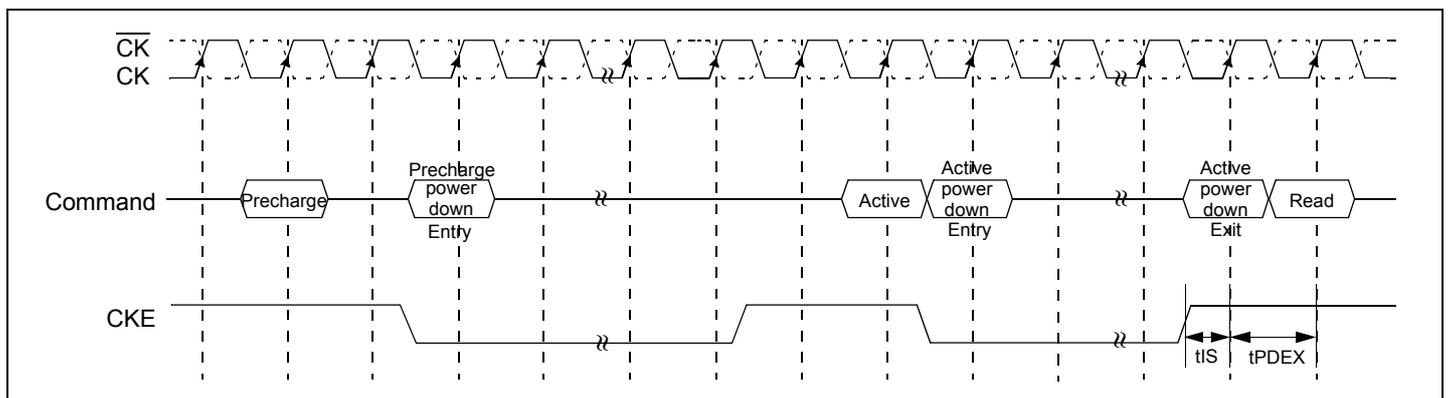
A self refresh command is defined by having \overline{CS} , \overline{RAS} , \overline{CAS} and \overline{CKE} held low with \overline{WE} high at the rising edge of the clock(CK). Once the self refresh command is initiated, \overline{CKE} must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except \overline{CKE} are ignored. Since \overline{CKE} is an SSTL_2 input, V_{ref} must be maintained during self refresh. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning \overline{CKE} high, asserting deselect or NOP command and then asserting \overline{CKE} high for longer than t_{XSRD} for locking of DLL.



1. Exit self refresh to bank active command, a write command can be applied as far as t_{RCD} is satisfied after any bank active command.
2. Exit self refresh to read command.

Power down

The power down mode is entered when \overline{CKE} is low and exited when \overline{CKE} is high. Once the power down mode is initiated, all of the receiver circuits except clock, \overline{CKE} and DLL circuit tree are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and \overline{CKE} should be set high at least $1t_{CK}+t_{IS}$ prior to row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot be remained in power down mode longer than the refresh period(Data retention time) of the device.



Power Up and Power Management on DDR Registered DIMMs

Background

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated $\overline{\text{RESET}}$ signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new $\overline{\text{RESET}}$ pin controls power dissipation on the module's registers and ensures that CKE and other SDRAM inputs are maintained at a valid 'low' level during power-up and self refresh. When $\overline{\text{RESET}}$ is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

The function for $\overline{\text{RESET}}$ is as follows:

Register Inputs				Register Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	Data in (D)	Data out (D)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal Input Conditions
L	x or Hi-Z	x or Hi-Z	x or Hi-Z	L

X : Don't Care
 Hi-Z : High Impedance
 Qo : Data latched at the previous crossing of CK rising and $\overline{\text{CK}}$ falling

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs-where they will remain until activated by a valid 'read' cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20MHz. When an input clock frequency of 20MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95MHz). If the clock input frequency drops below 20MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are made High-Z, and the differential inputs are powered down-resulting in a total PLL current consumption of less than 1mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or G pin) unnecessary, and it is tied inactive on the DIMM.

This application note describes the required and optional system sequences associated with the DDR Registered DIMM $\overline{\text{RESET}}$ function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with $\overline{\text{RESET}}$ - Required

1. The system sets $\overline{\text{RESET}}$ at a valid low level.

This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.

2. The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.

3. Stabilization of Clocks to the SDRAM

The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 usec prior to SDRAM operation.

4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).

CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.

5. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.

The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).

6. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time ($t(\text{ACT})$), from asynchronous switching of RESET from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM documentation.

7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-approved initialization sequence).

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks powered off) - Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the $\overline{\text{RESET}}$ pin, as this can reduce register power consumption (RESET low deactivates register CK and $\overline{\text{CK}}$, data input receivers, and data output drivers).

1. The system applies Self Refresh entry command.
(CKE ->Low, CS->Low, RAS->Low, CAS->Low, WE->High)

Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Care with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level.

This input condition forces all register outputs to a low state, independent of the condition on the register inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required.

3. The system turns off clock inputs to the DIMM. (Optional)

a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock inputs to both the SDRAMs and the registers. This must be done after the $\overline{\text{RESET}}$ deactivate time of the register ($t(\text{INACT})$). The deactivate time defines the time in which the clocks and the control and address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied and is specified in the register and DIMM documentation.

b. The system may release DIMM address and control inputs to High-Z.

This can be done after the $\overline{\text{RESET}}$ deactivate time of the register. The deactivate time defines the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied. It is highly recommended that CKE continue to remain low during this operation.

4. The DIMM is in lowest power Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks powered off) - Optional

1. Stabilization of Clocks to the SDRAM.

The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches ~20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds.

2. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC Self Refresh Exit sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs, to be consistent with the state of the register outputs.

3. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.

The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, $\overline{\text{RESET}}$ timing relationship to a specific clock edge is not required (during this period, register inputs must remain stable).

4. The system must maintain stable register inputs until normal register operation is attained.

The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 2. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time ($t(\text{ACT})$), from asynchronous switching of RESET from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM documentation.

5. System can begin the JEDEC-defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks running) - Optional

Although keeping the clocks running increases power consumption from the on-DIMM PLL during self refresh, this is an alternate operating mode for these DIMMs.

1. System enters Self Refresh entry command.
($\overline{\text{CKE}}$ ->Low, $\overline{\text{CS}}$ ->Low, $\overline{\text{RAS}}$ ->Low, $\overline{\text{CAS}}$ ->Low, $\overline{\text{WE}}$ ->High)

Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Cares - with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level.
This input condition forces all register outputs to a low state, independent of the condition on the data and clock register inputs, and ensures that CKE is a stable low-level at the DDR SDRAMs.

3. The system may release DIMM address and control inputs to High-Z.

This can be done after the $\overline{\text{RESET}}$ deactivate time of the register ($t(\text{INACT})$). The deactivate time describes the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied. It is highly recommended that CKE continue to remain low during the operation.

4. The DIMM is in a low power, Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks running) - Optional

1. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).

CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the Self Refresh Exit sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.

2. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.
The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, it does not need to be tied to a particular clock edge (during this period, register inputs must continue to remain stable).

3. The system must maintain stable register inputs until normal register operation is attained. The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 1. It is also a functional requirement that the registers maintain a low state at the CKE outputs in order to guarantee that the DDR SDRAMs continue to receive a low level on CKE. This activation time, from asynchronous switching of $\overline{\text{RESET}}$ from low to high, until the registers are stable and ready to accept an input signal, is $t(\text{ACT})$ as specified in the register and DIMM documentation.

4. The system can begin JEDEC defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry/Exit ($\overline{\text{RESET}}$ high, clocks running) - Optional

As this sequence does not involve the use of the $\overline{\text{RESET}}$ function, the JEDEC standard SDRAM specification explains in detail the method for entering and exiting Self Refresh for this case.

Self Refresh Entry ($\overline{\text{RESET}}$ high, clocks powered off) - Not Permissible

In order to maintain a valid low level on the register output, it is required that either the clocks be running and the system drive a low level on CKE, or the clocks are powered off and $\overline{\text{RESET}}$ is asserted low according to the sequence defined in this application note. In the case where $\overline{\text{RESET}}$ remains high and the clocks are powered off, the PLL drives a High-Z clock input into the register clock input. Without the low level on $\overline{\text{RESET}}$ an unknown DIMM state will result.

Functional Truth Table

Current State	CS	RAS	CAS	WE	Address	Command	Action
PRECHARGE STANDBY	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*4
	L	L	L	H	X	Refresh	AUTO-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ACTIVE STANDBY	L	H	H	L	X	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	L	H	H	L	X	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Pre- charge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Pre- charge*3
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst With DM=High, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE*6 (READA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	*6
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	*6
	L	L	H	L	BA, A10	PRE/PREA	*6
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	CS	RAS	CAS	WE	Address	Command	Action
WRITE with AUTO RECHARGE*7 (WRITEA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	*7
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	*7
	L	L	H	H	BA, RA	Active	*7
	L	L	H	L	BA, A10	PRE/PREA	*7
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING (DURING tRP)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING (FROM ROW ACTIVE TO tRCD)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING (DURING tWR OR tCDLR)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	H	BA, CA, A10	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	CKEn-1	CKEn	CS	RAS	CAS	WE	Add	Action
SELF-REFRESHING* ⁸	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOOperation(Maintain Self-Refresh)
POWER DOWN	L	H	X	X	X	X	X	Exit Power Down(Idle after tPDEX)
	L	L	X	X	X	X	X	NOOperation(Maintain Power Down)
ALL BANKS IDLE* ⁹	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
L	X	X	X	X	X	X	X	Refer to Current State=Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table

ABBREVIATIONS :

H=High Level, L=Low level, X=Don't Care

Note :

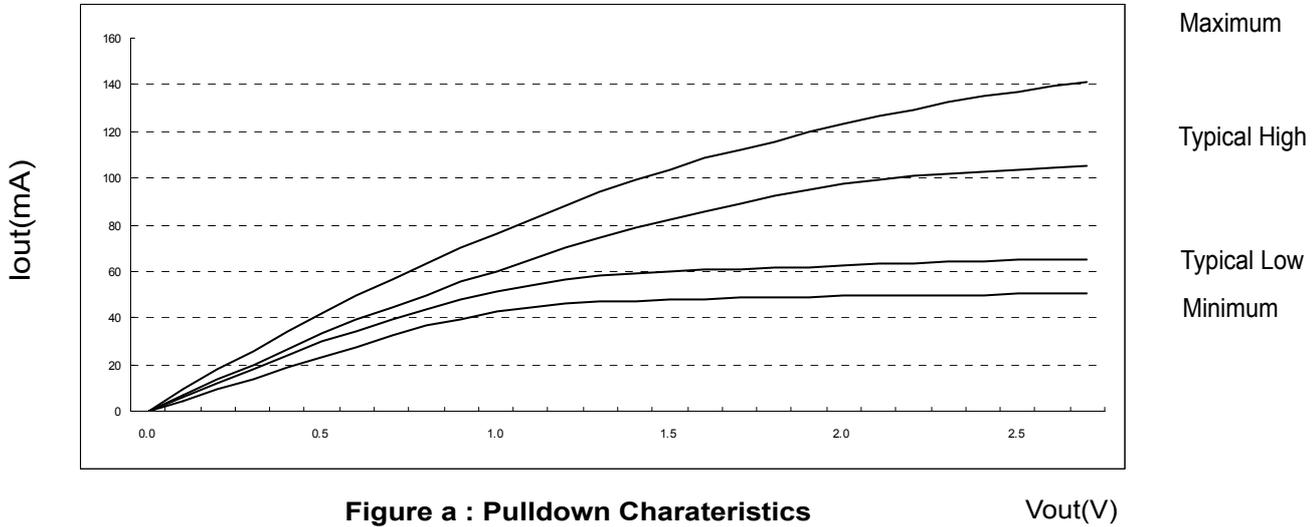
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around and write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Refer to "Read with Auto Precharge" in page 85 for detailed information.
7. Refer to "Write with Auto Precharge" in page 86 for detailed information.
8. CKE Low to High transition will re-enable CK, \overline{CK} and other inputs asynchronously. A minimum setup time must be satisfied before issuing any command other than EXIT.
9. Power-Down and Self-Refresh can be entered only from All Bank Idle state.
10. Vref must be maintained during self refresh operation.

ILLEGAL = Device operation and/or data integrity are not guaranteed.

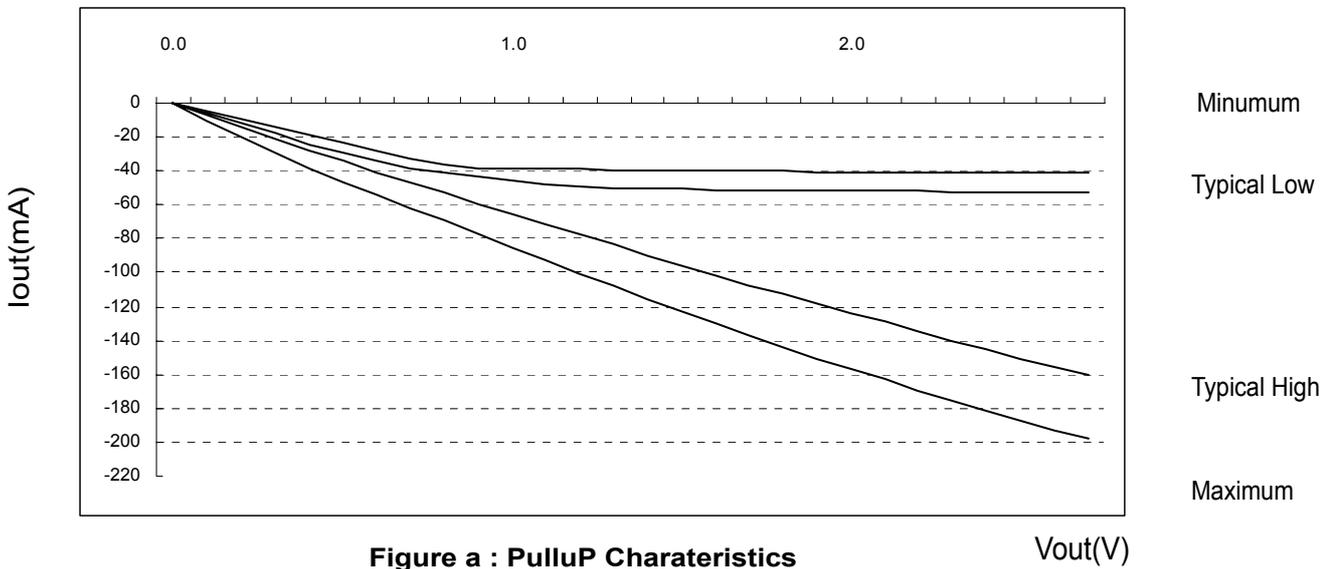
IBIS: I/V Characteristics for Input and Output Buffers

Normal strength driver

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.
2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.



3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.
4. The Full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure b.



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to $V_{DDQ}/2$
6. The Full variation in the ratio of the nominal pullup to pulldown current should be unity $\pm 10\%$, for device drain to source voltages from 0 to $V_{DDQ}/2$

Voltage (V)	Pulldown Current (mA)				pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-41.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Temperature (Tambient)

Typical 25°C
 Minimum 70°C
 Maximum 0°C

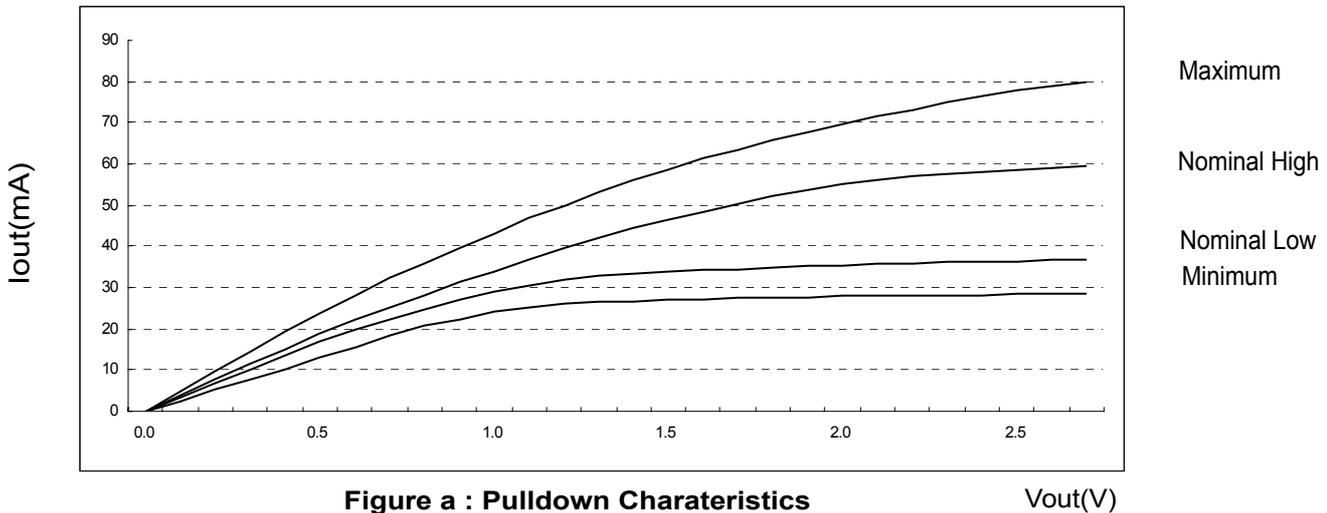
Vdd/Vddq

Typical 2.5V
 Minimum 2.3V
 Maximum 2.7V

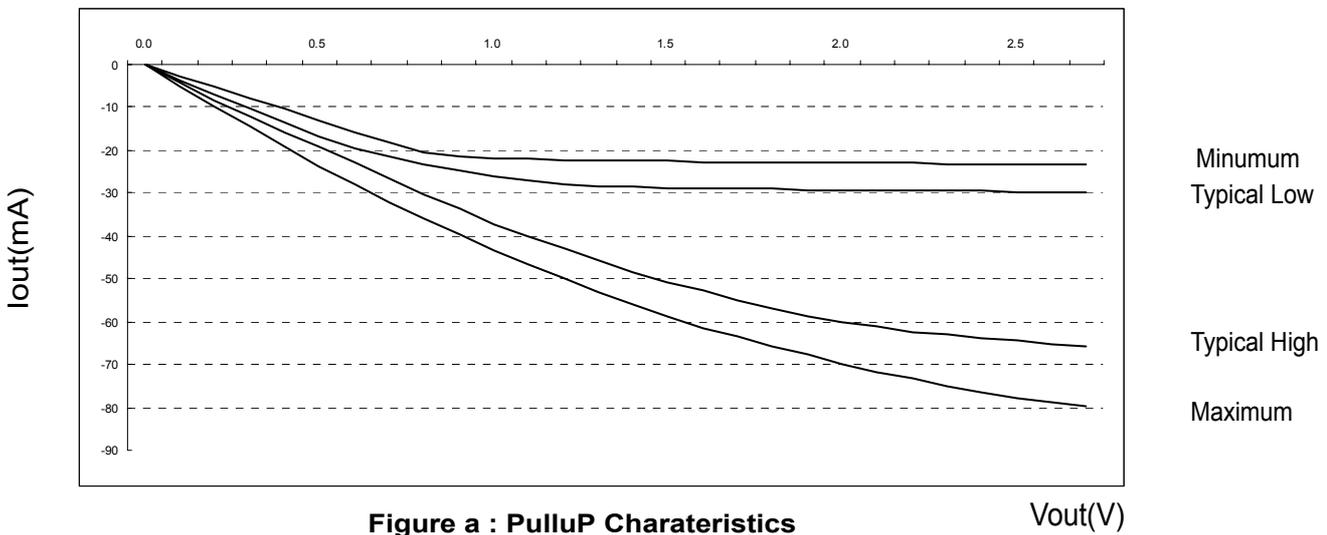
The above characteristics are specified under best, worst and normal process variation/conditions

Half Strength Driver

1. The typical pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.
2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.



3. The typical pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.
4. The Full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure b.



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to $V_{DDQ}/2$
6. The Full variation in the ratio of the nominal pullup to pulldown current should be unity $\pm 10\%$, for device drain to source voltages from 0 to $V_{DDQ}/2$

Voltage (V)	Pulldown Current (mA)				pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6	19.6	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

Temperature (Tambient)

Typical 25°C
 Minimum 70°C
 Maximum 0°C

Vdd/Vddq

Typical 2.5V
 Minimum 2.3V
 Maximum 2.7V

The above characteristics are specified under best, worst and normal process variation/conditions

Test Condition

DDR SDRAM IDD SPEC Items and Test Conditions

(V_{DD}=2.7V, T = 10°C)

Conditions	Symbol
Operating current - One bank Active-Precharge; t _{RC} =t _{RCmin} ; DQ,DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	IDD0
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	IDD1
Precharge power-down standby current; All banks idle; power - down mode; CKE = <V _{IL} (max); V _{in} = V _{ref} for DQ,DQS and DM	IDD2P
Precharge Floating standby current; CS# > =V _{IH} (min);All banks idle; CKE > = V _{IH} (min); Address and other control inputs changing once per clock cycle; V _{in} = V _{ref} for DQ,DQS and DM	IDD2F
Precharge Quiet standby current; CS# > = V _{IH} (min); All banks idle; CKE > = V _{IH} (min); Address and other control inputs stable with keeping >= V _{IH} (min) or =<V _{IL} (max); V _{in} = V _{ref} for DQ ,DQS and DM	IDD2Q
Active power - down standby current ; one bank active; power-down mode; CKE=< V _{IL} (max); V _{in} = V _{ref} for DQ,DQS and DM	IDD3P
Active standby current; CS# >= V _{IH} (min); CKE>=V _{IH} (min); one bank active; active - precharge; t _{RC} =t _{RASmax} ; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; 50% of data changing at every burst; I _{out} = 0 m A	IDD4R
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W
Auto refresh current; t _{RC} = t _{RFC} (min) - 8*t _{CK} for DDR200 at 100Mhz, 10*t _{CK} for DDR266A & DDR266B at 133Mhz and 12*t _{CK} for DDR333; distributed refresh	IDD5
Self refresh current; CKE =< 0.2V; External clock should be on; t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B and 166Mhz for DDR333	IDD6
Orerating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7A

Detailed test conditions for DDR SDRAM IDD1 & IDD7

IDD1 : Operating current: One bank operation

1. Only one bank is accessed with $t_{RC}(\min)$, Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle.
 $I_{out} = 0\text{mA}$

2. Timing patterns

- DDR200(100Mhz, CL=2) : $t_{CK} = 10\text{ns}$, CL=2, BL=4, $t_{RCD} = 2*t_{CK}$, $t_{RAS} = 5*t_{CK}$
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
- DDR266B(133Mhz, CL=2.5) : $t_{CK} = 7.5\text{ns}$, CL=2.5, BL=4, $t_{RCD} = 3*t_{CK}$, $t_{RC} = 9*t_{CK}$, $t_{RAS} = 5*t_{CK}$
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
- DDR266A (133Mhz, CL=2) : $t_{CK} = 7.5\text{ns}$, CL=2, BL=4, $t_{RCD} = 3*t_{CK}$, $t_{RC} = 9*t_{CK}$, $t_{RAS} = 5*t_{CK}$
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
- DDR333(166Mhz, CL=2.5) : $t_{CK}=6\text{ns}$, CL=2.5, BL=4, $t_{RCD}=10*t_{CK}$, $t_{RAS}=7*t_{CK}$
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

IDD7A : Operating current: Four bank operation

1. Four banks are being interleaved with $t_{RC}(\min)$, Burst Mode, Address and Control inputs on NOP edge are not changing. $I_{out} = 0\text{mA}$

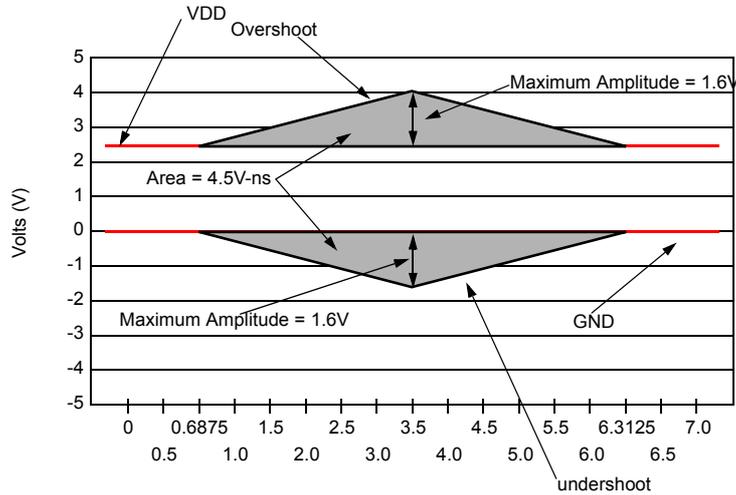
2. Timing patterns

- DDR200(100Mhz, CL=2) : $t_{CK} = 10\text{ns}$, CL=2, BL=4, $t_{RRD} = 2*t_{CK}$, $t_{RCD} = 3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
*50% of data changing at every burst
- DDR266B(133Mhz, CL=2.5) : $t_{CK} = 7.5\text{ns}$, CL=2.5, BL=4, $t_{RRD} = 2*t_{CK}$, $t_{RCD} = 3*t_{CK}$
Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*50% of data changing at every burst
- DDR266A (133Mhz, CL=2) : $t_{CK} = 7.5\text{ns}$, CL=2, BL=4, $t_{RRD} = 2*t_{CK}$, $t_{RCD} = 3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*50% of data changing at every burst
- DDR333(166Mhz, CL=2.5) : $t_{CK}=6\text{ns}$, CL=2.5, BL=4, $t_{RRD}=2*t_{CK}$, $t_{RCD}=3*t_{CK}$, Read with autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

Overshoot/Undershoot specification for Address and Control Pins

Parameter	Specification	Notes
Maximum peak amplitude allowed for overshoot (See Figure 1):	1.6 V	1,2,3
Maximum peak amplitude allowed for undershoot (See Figure 1):	1.6 V	1,2,3
The area between the overshoot signal and VDD must be less than or equal to (See Figure 1):	4.5 V-ns	1,2,3
The area between the undershoot signal and GND must be less than or equal to (See Figure 1):	4.5 V-ns	1,2,3

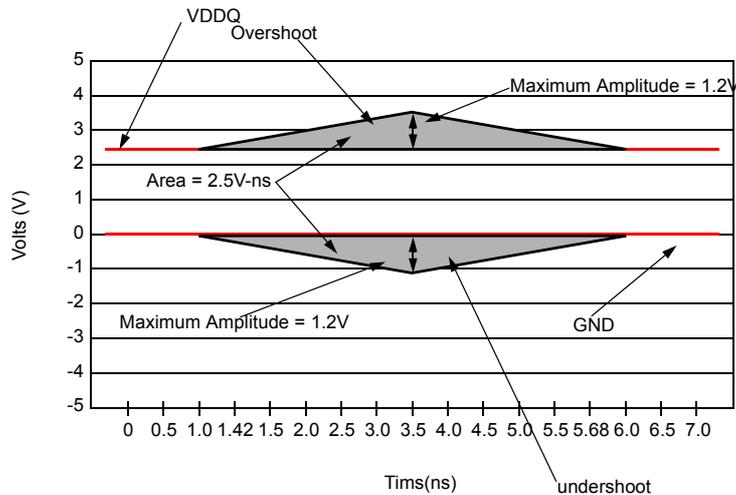


Notes:

1. This specification is intended for only DDR200, DDR266A and DDR266B devices.
2. This specification is intended for only devices with NO clamp protection
3. This compliance is to be verified by design only.

Overshoot/Undershoot specification for Data Pins

Parameter	Specification	Notes
Maximum peak amplitude allowed for overshoot (See Figure 2):	1.2 V	1,2,3
Maximum peak amplitude allowed for undershoot (See Figure 2):	1.2 V	1,2,3
The area between the overshoot signal and VDD must be less than or equal to (See Figure 2):	2.5 V-ns	1,2,3
The area between the undershoot signal and GND must be less than or equal to (See Figure 2):	2.5 V-ns	1,2,3



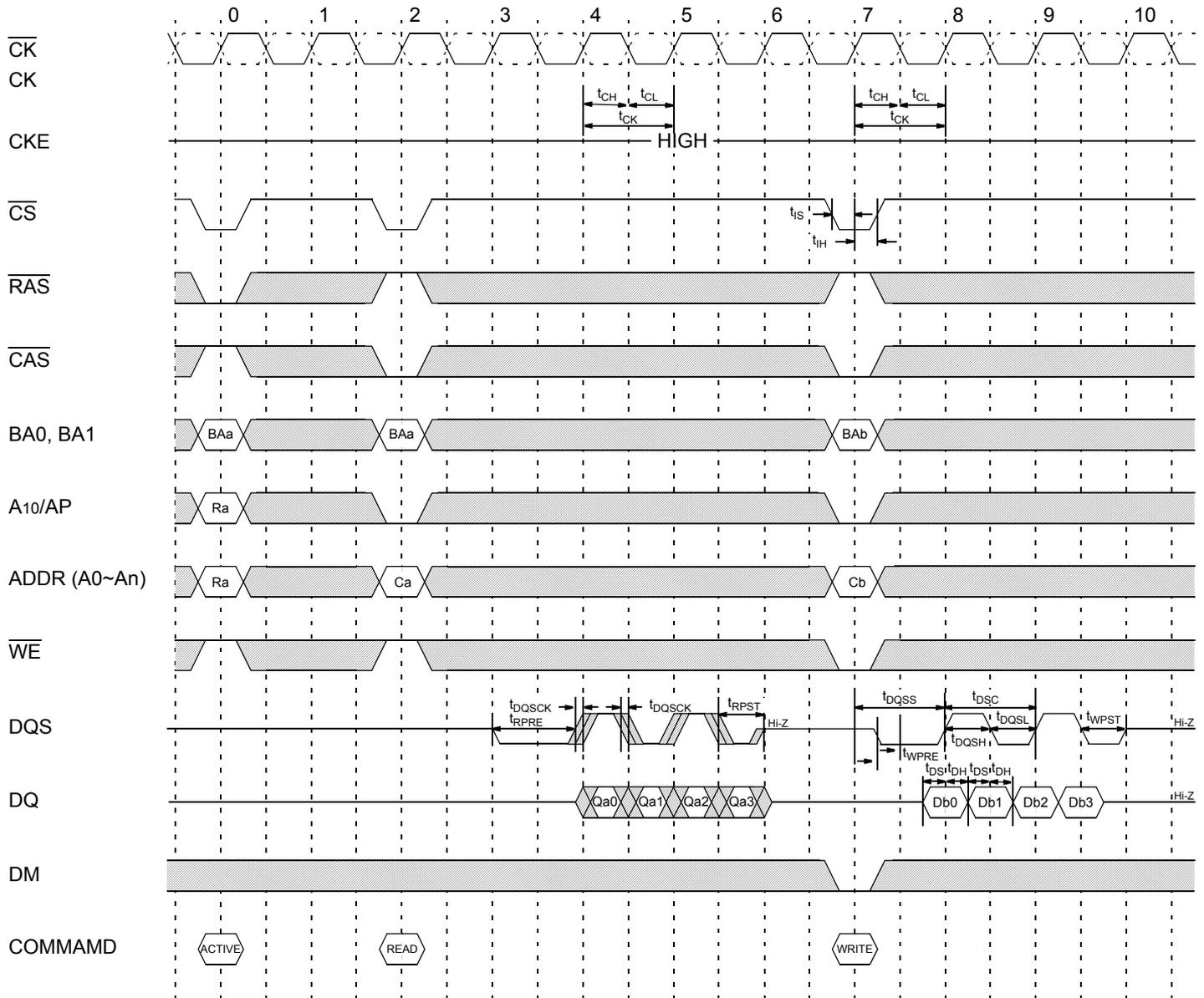
Notes:

1. This specification is intended for only DDR200, DDR266A and DDR266B devices.
2. This specification is intended for only devices with NO clamp protection
3. This compliance is to be verified by design only.

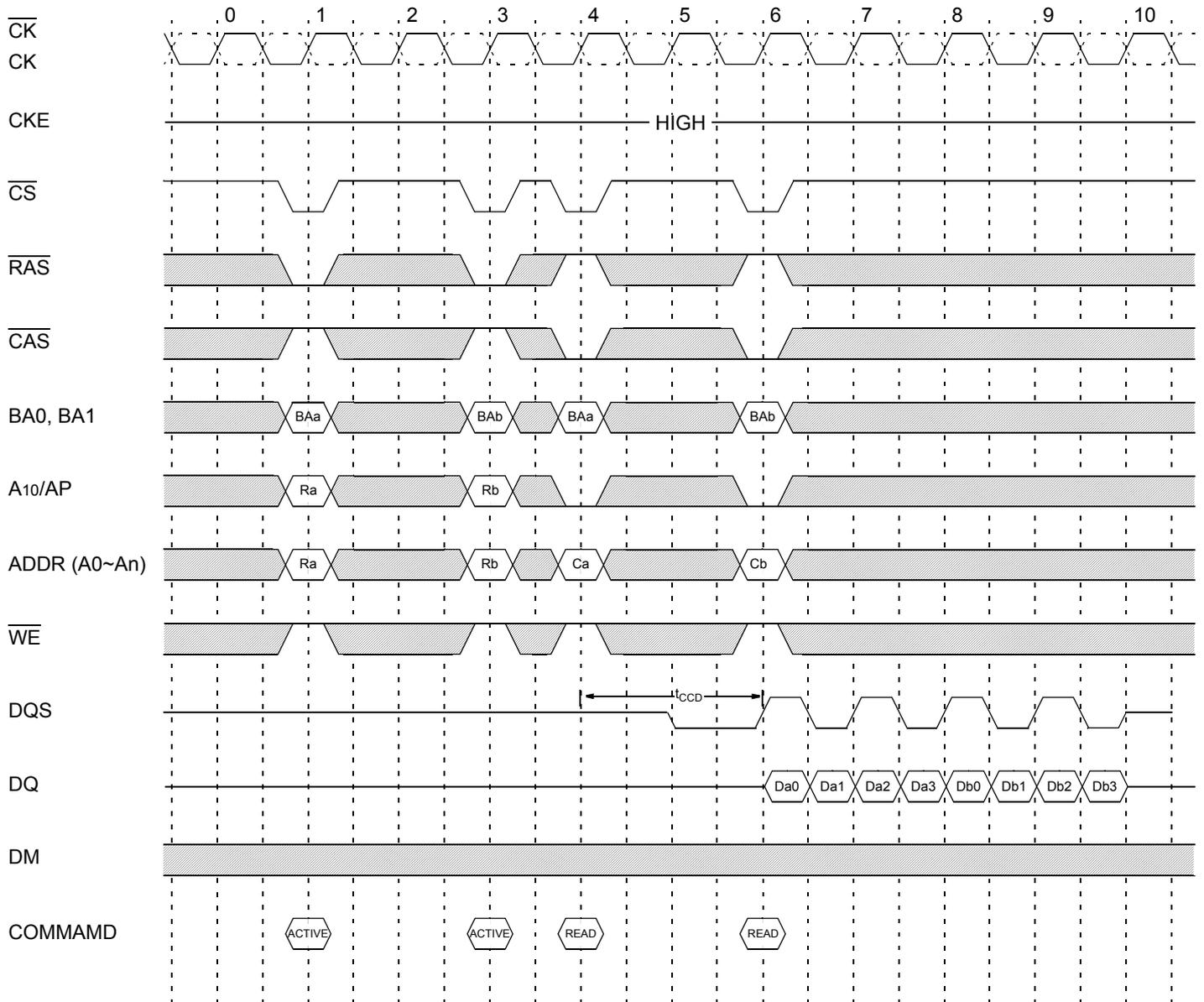
Timing Diagram

Timing Diagram

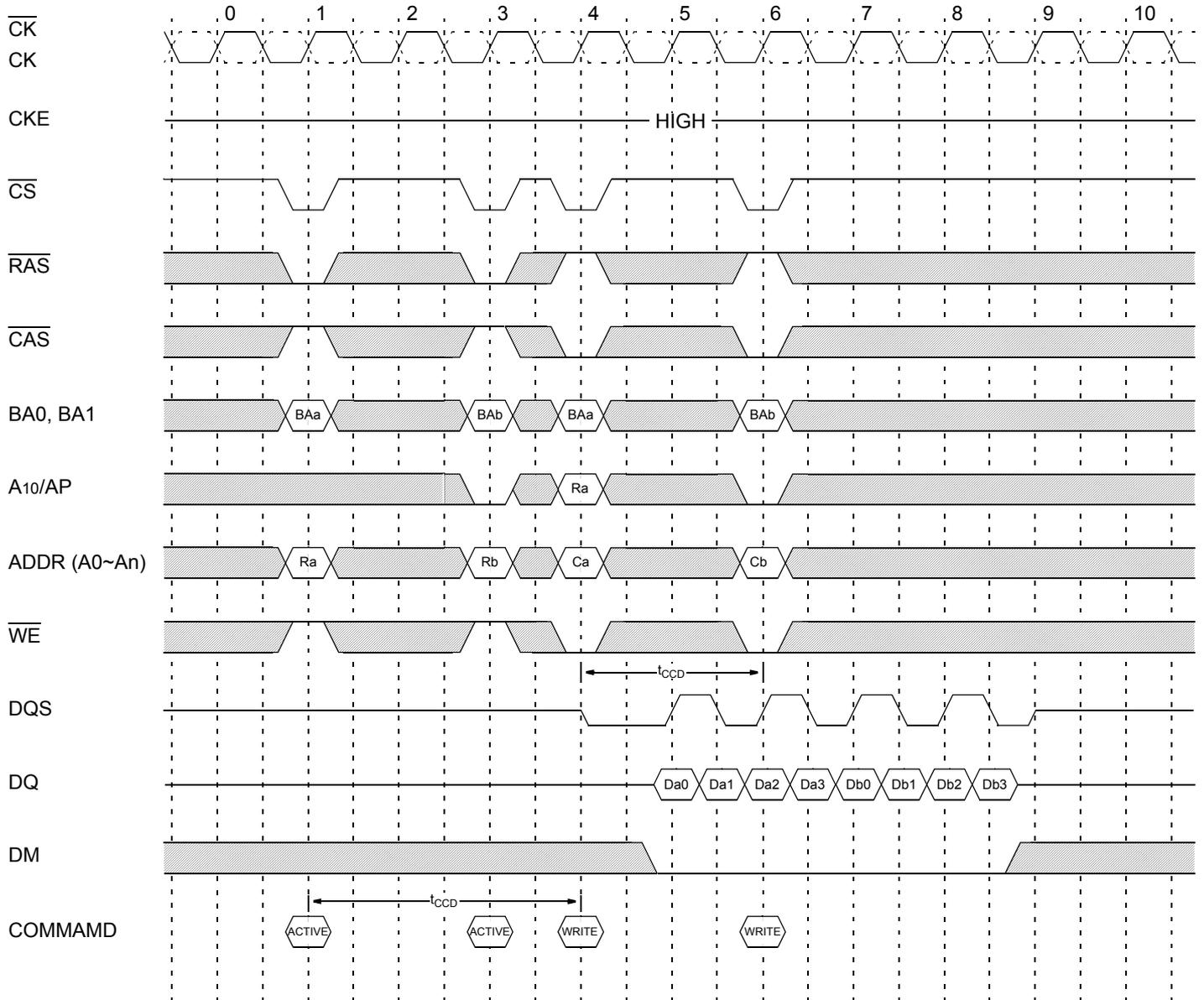
Basic Timing (Setup, Hold and Access Time @BL=4, CL=2)



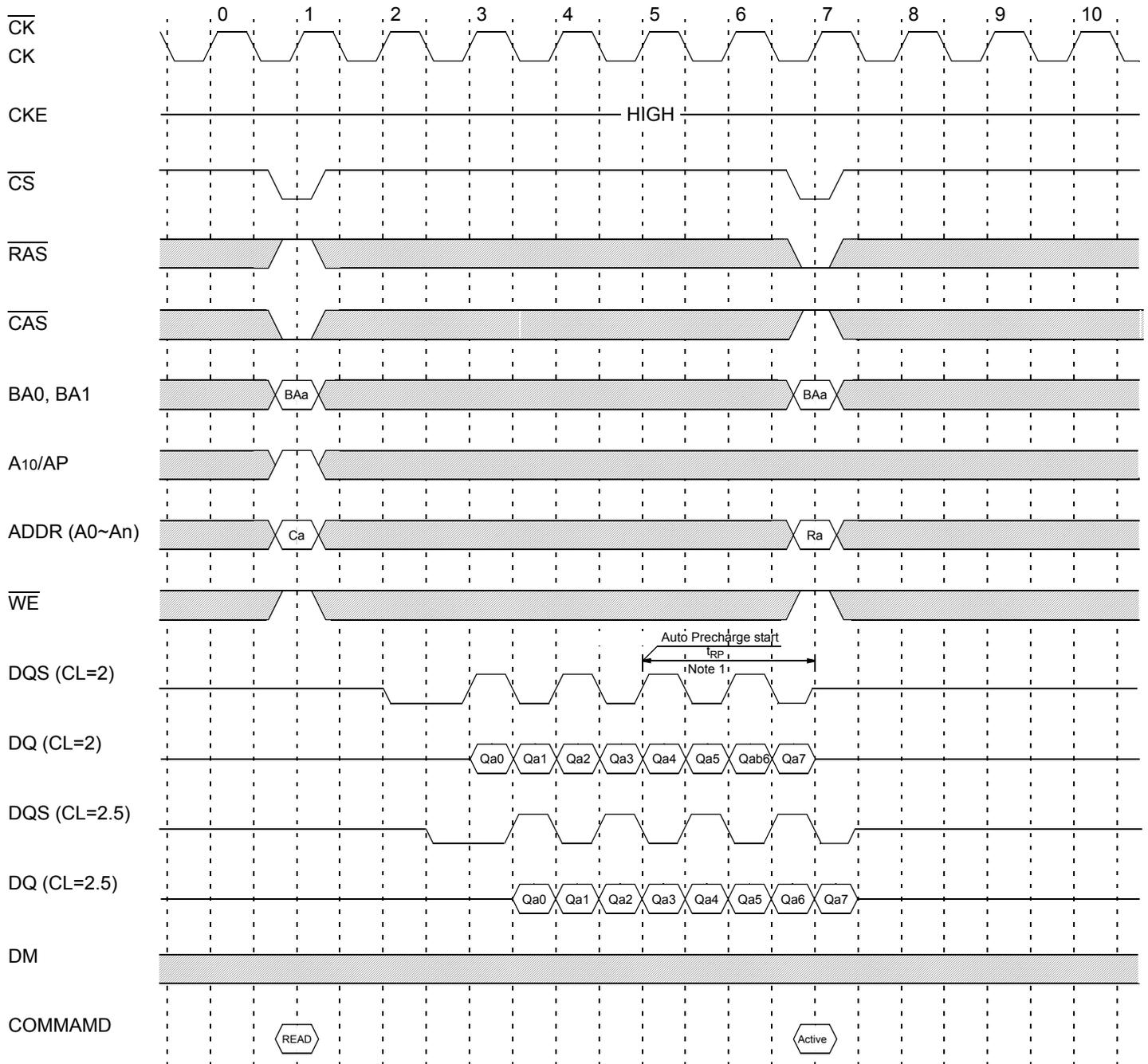
Multi Bank Interleaving READ (@BL=4, CL=2)



Multi Bank Interleaving WRITE (@BL=4)

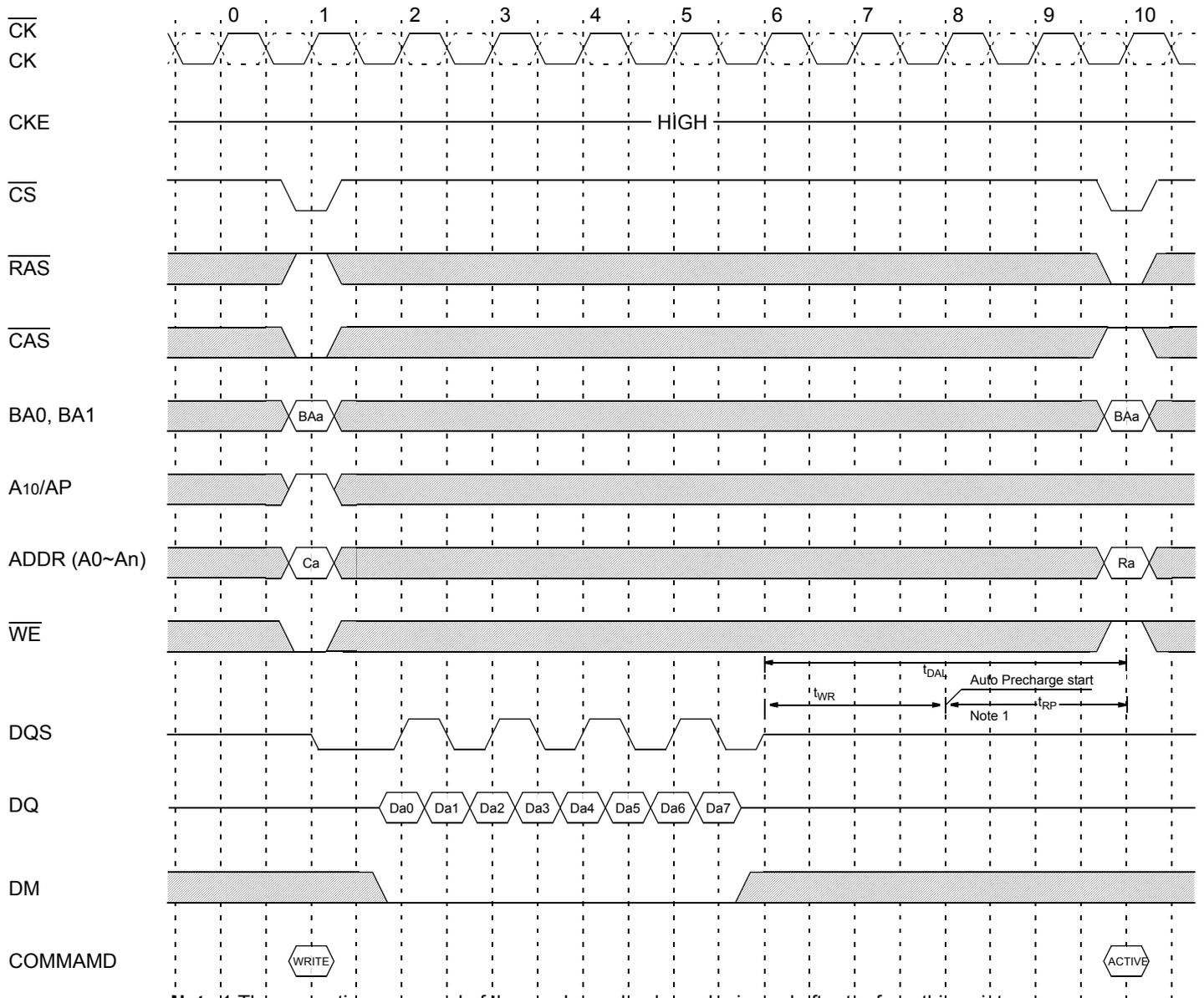


Read with Auto Precharge (@BL=8)



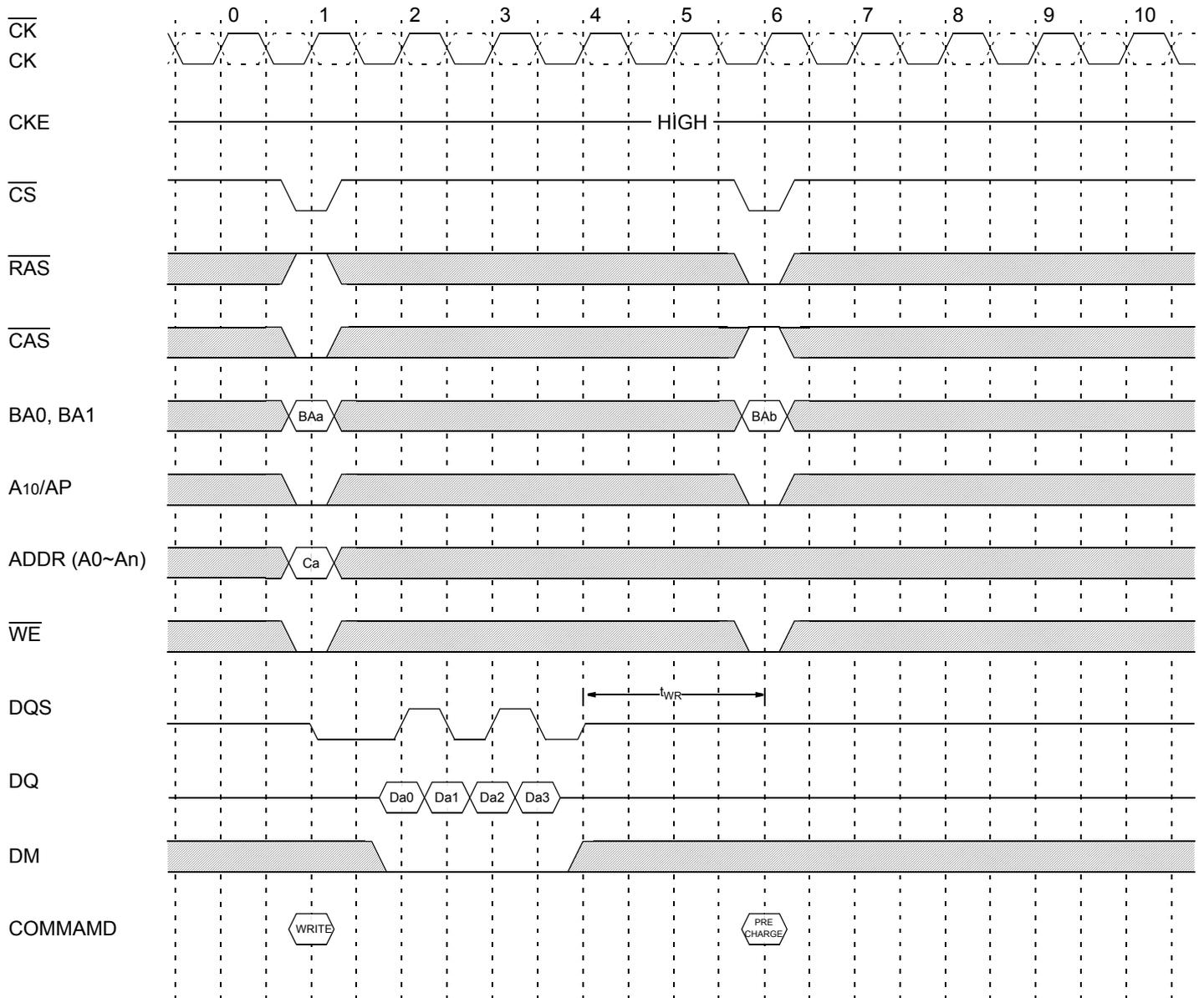
Note 1 The row active command of the precharge bank can be issued after t_{RP} from this point
 The new read/write command of another activated bank can be issued from this point
 At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

Write with Auto Precharge (@BL=8)

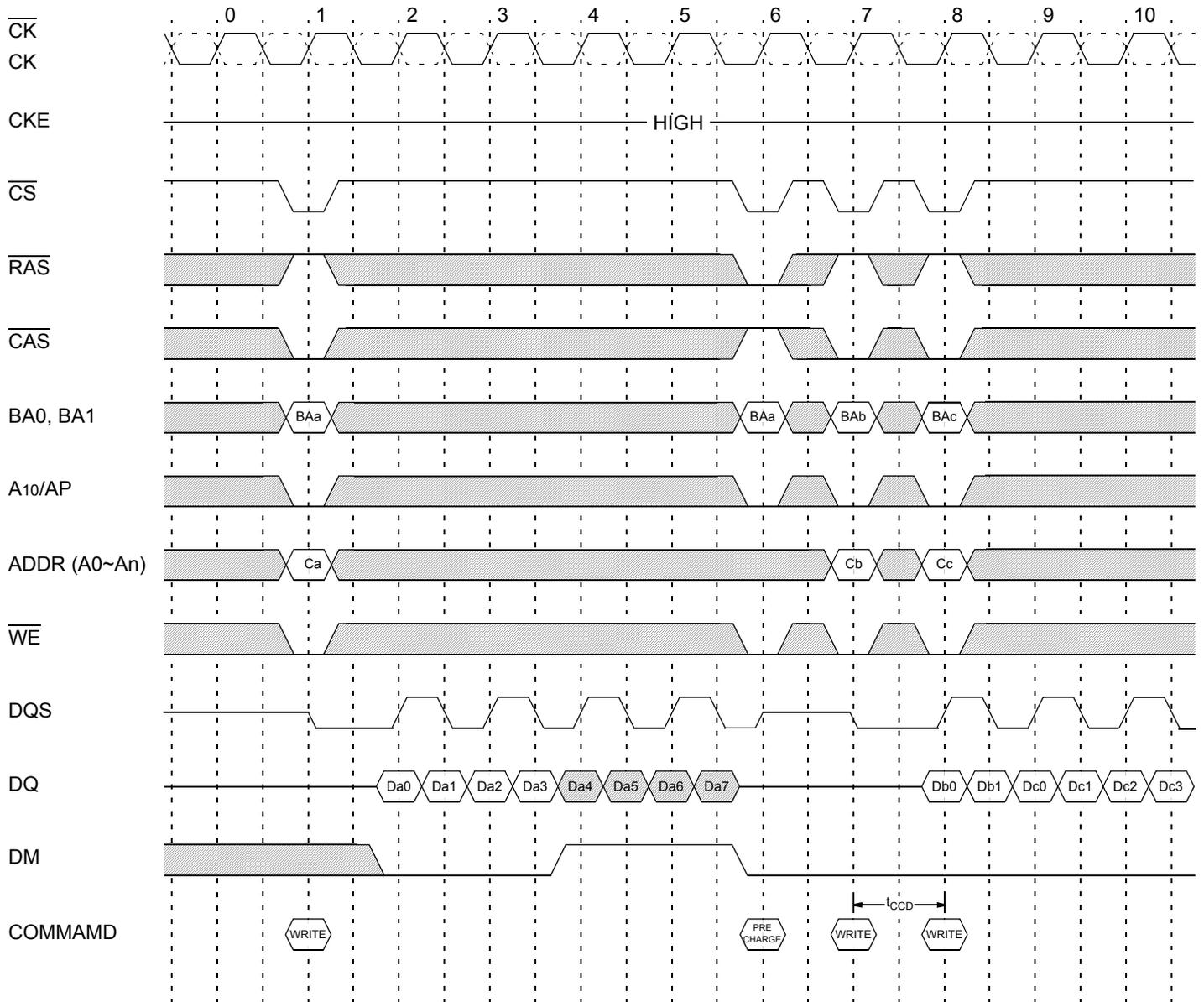


Note 1 The row active command of the precharge bank can be issued after t_{RP} from this point
 The new read/write command of another activated bank can be issued from this point
 At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

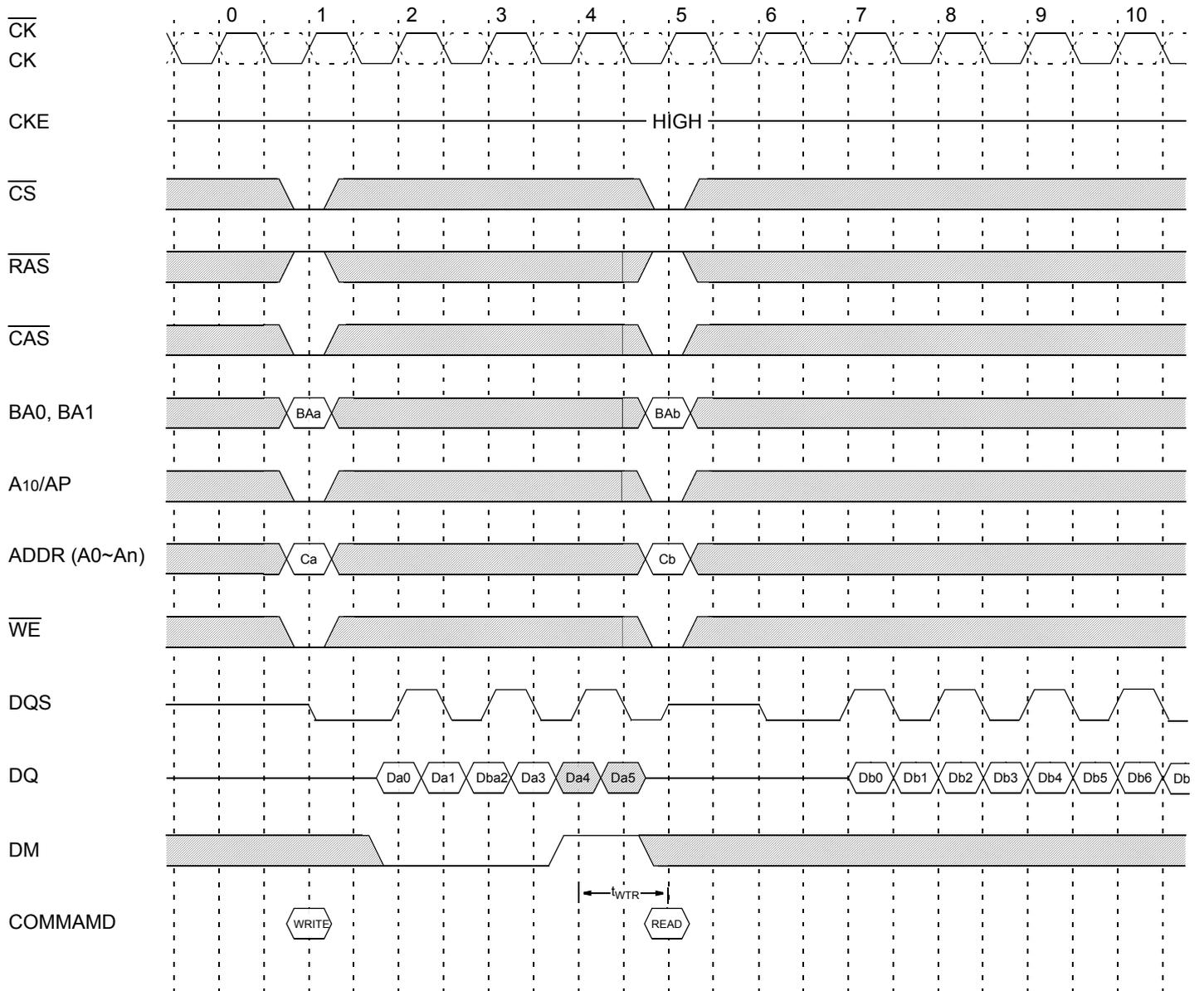
Write followed by Precharge (@BL=4)



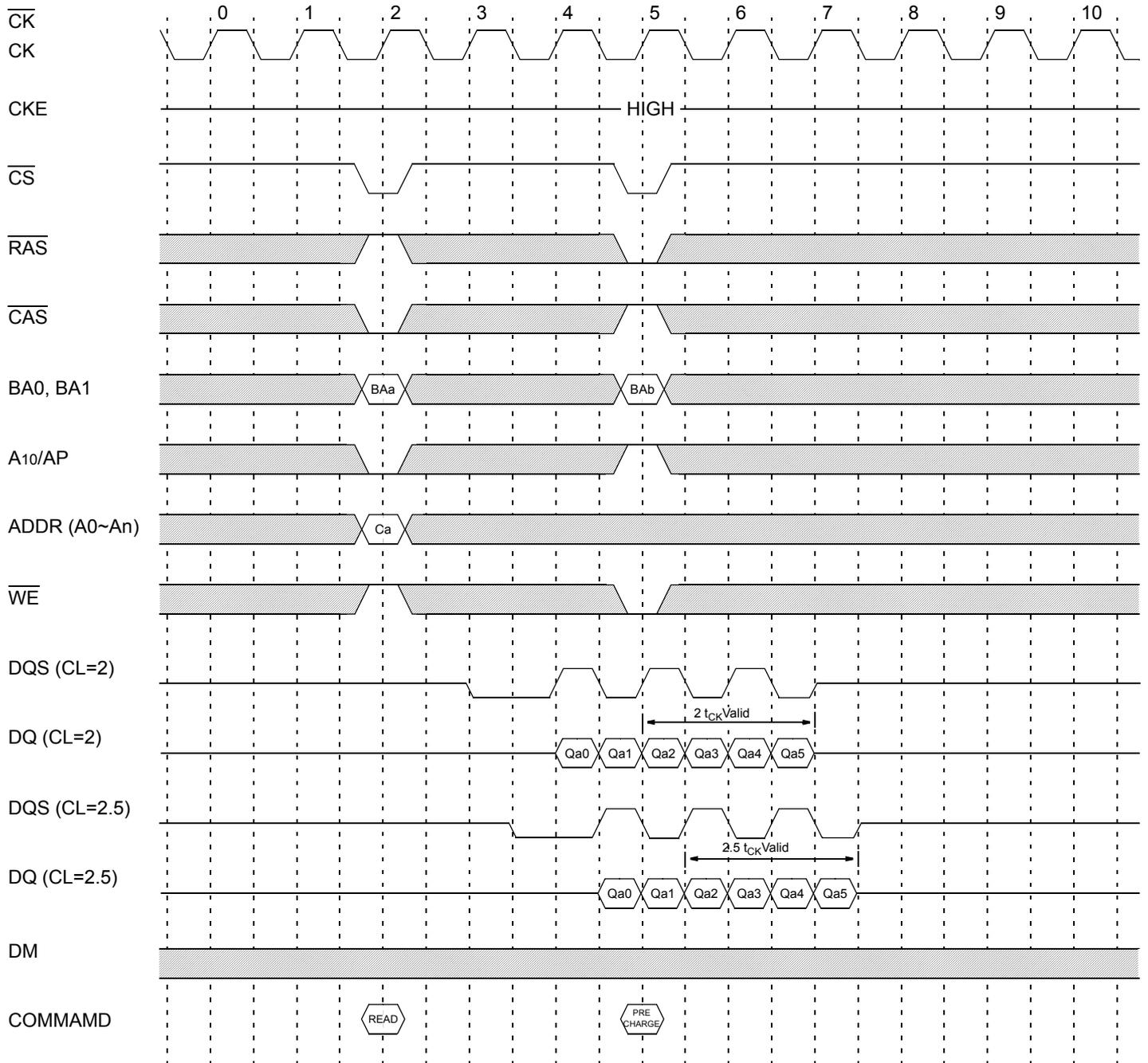
Write Interrupted by Precharge & DM (@BL=8)



Write Interrupted by a Read (@BL=8, CL=2)



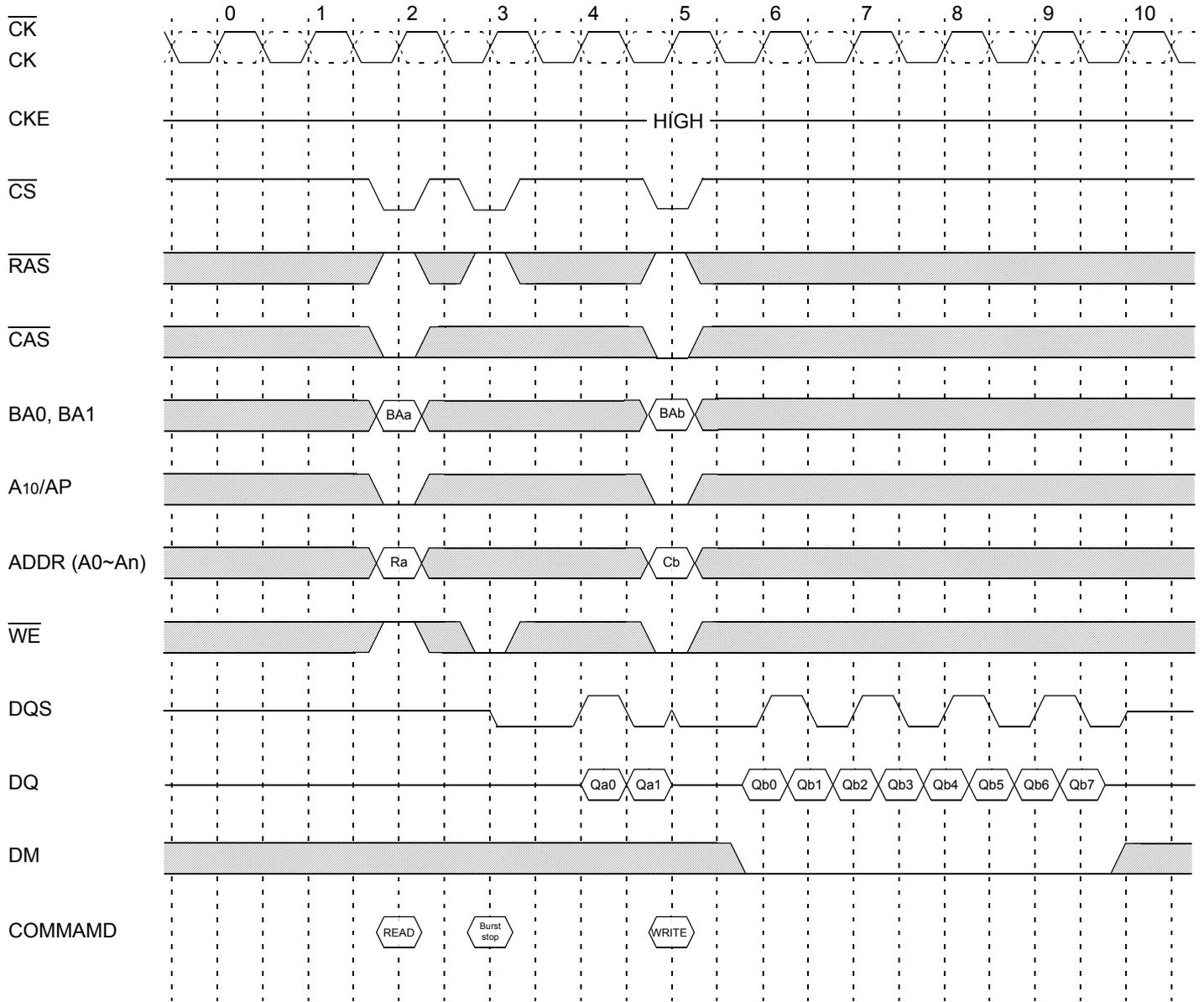
Read Interrupted by Precharge (@BL=8)



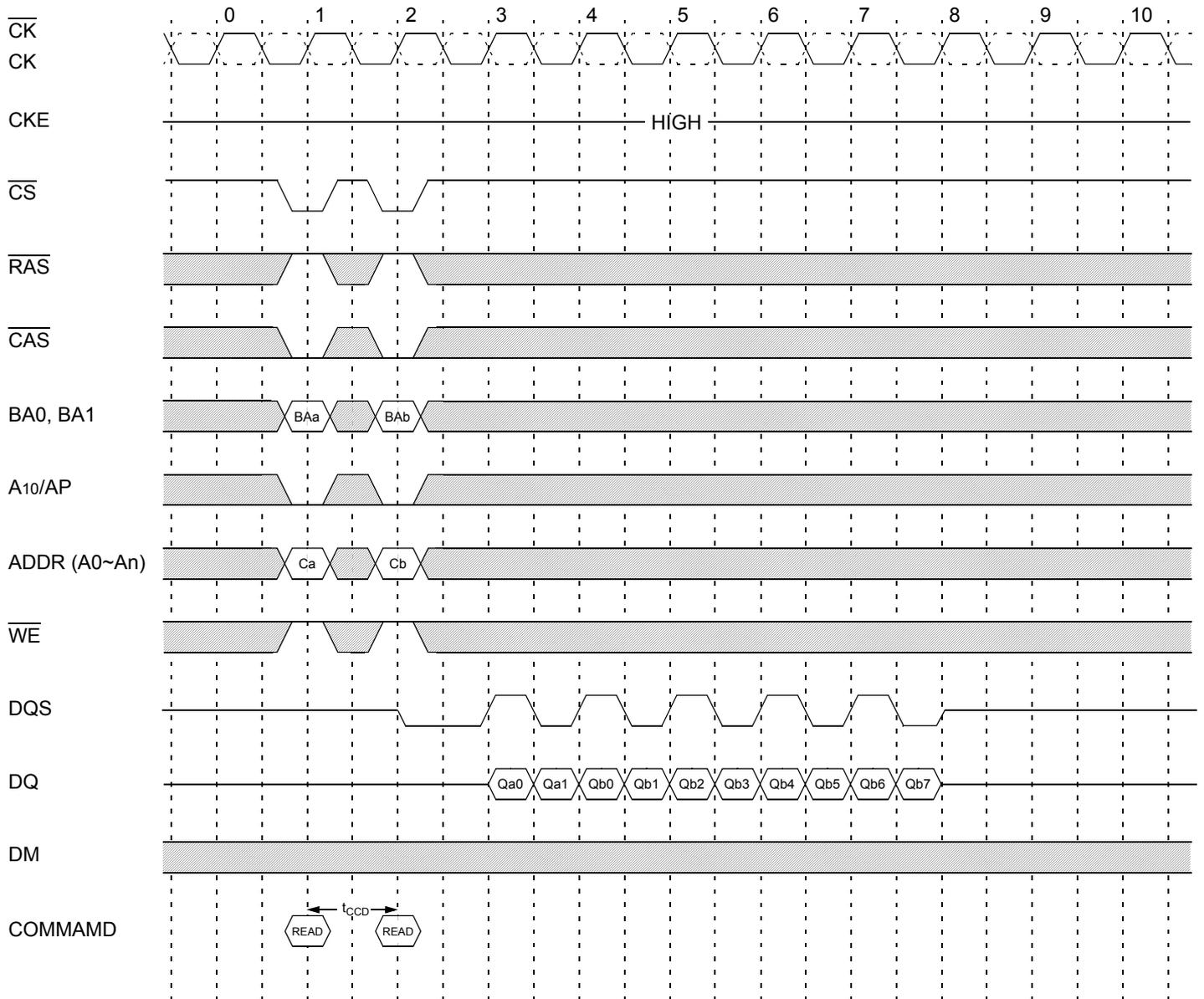
When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.

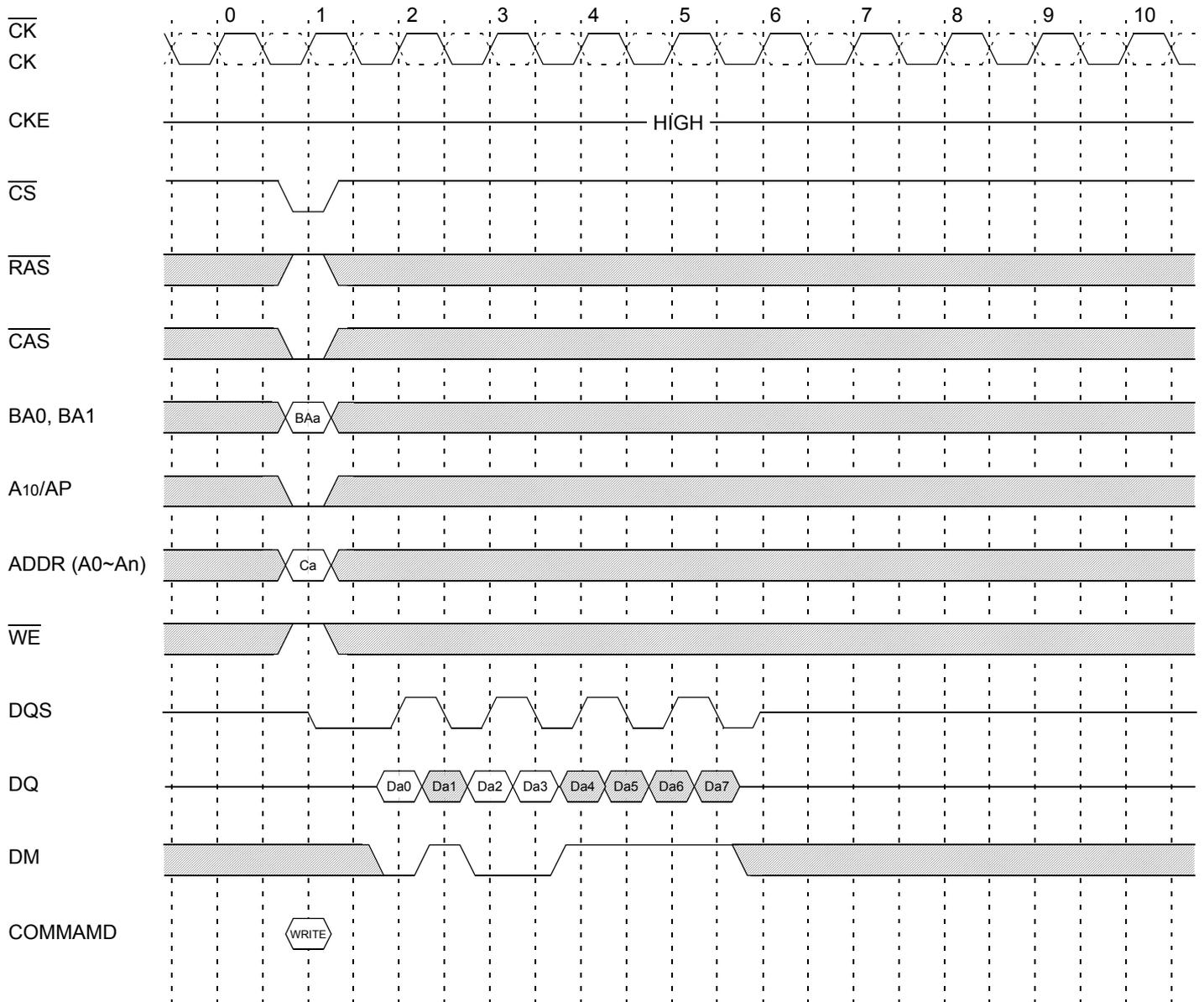
Read Interrupted by a Write & Burst Stop (@BL=8, CL=2)



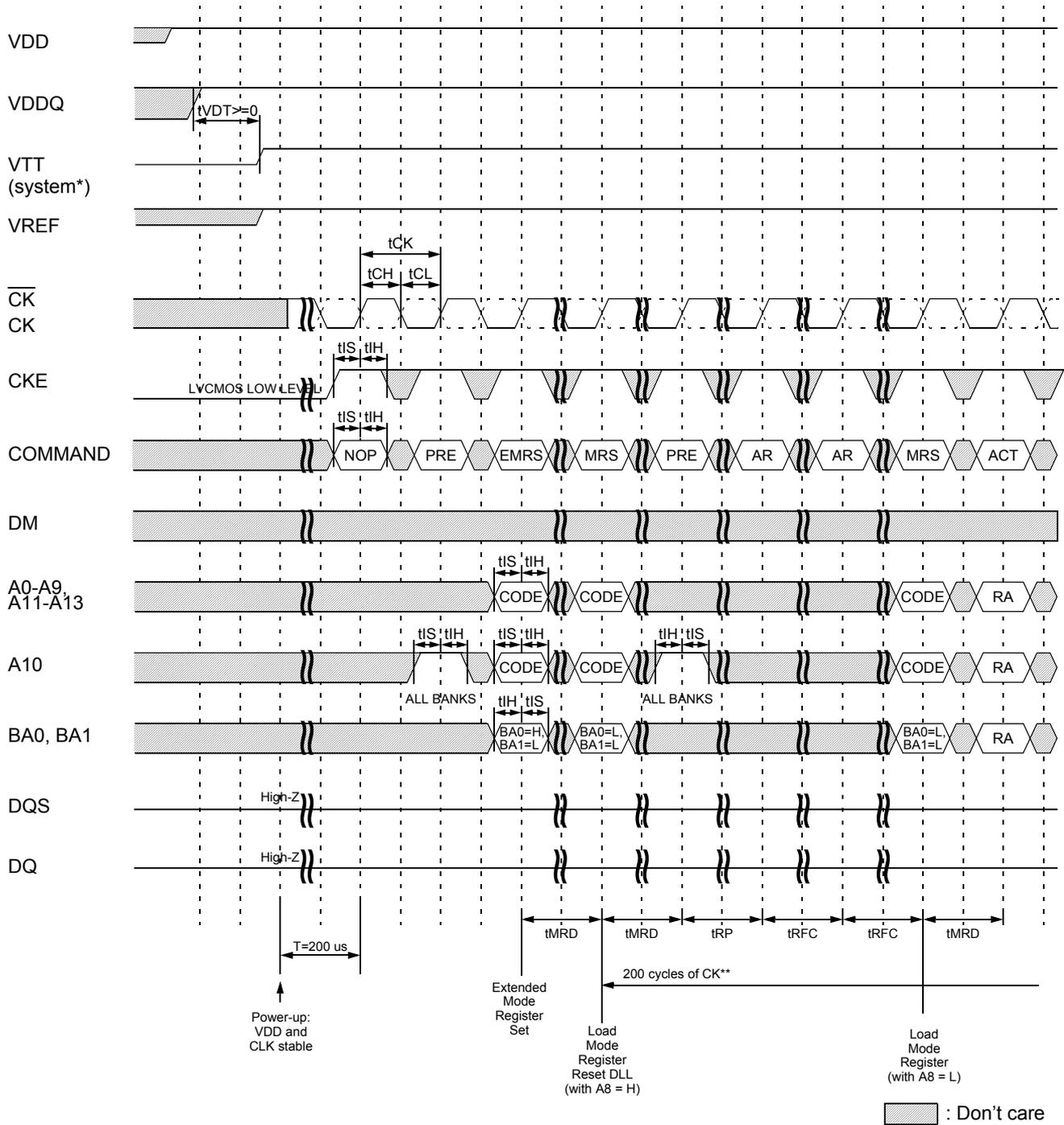
Read Interrupted by a Read (@BL=8, CL=2)



DM Function (@BL=8) only for write



Power up & Initialization Sequence(based on DDR400)



* = VTT is not applied directly to the device, however t_{VDT} must be greater than or equal to avoid latch-up.

** = t_{MRD} is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied. The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

