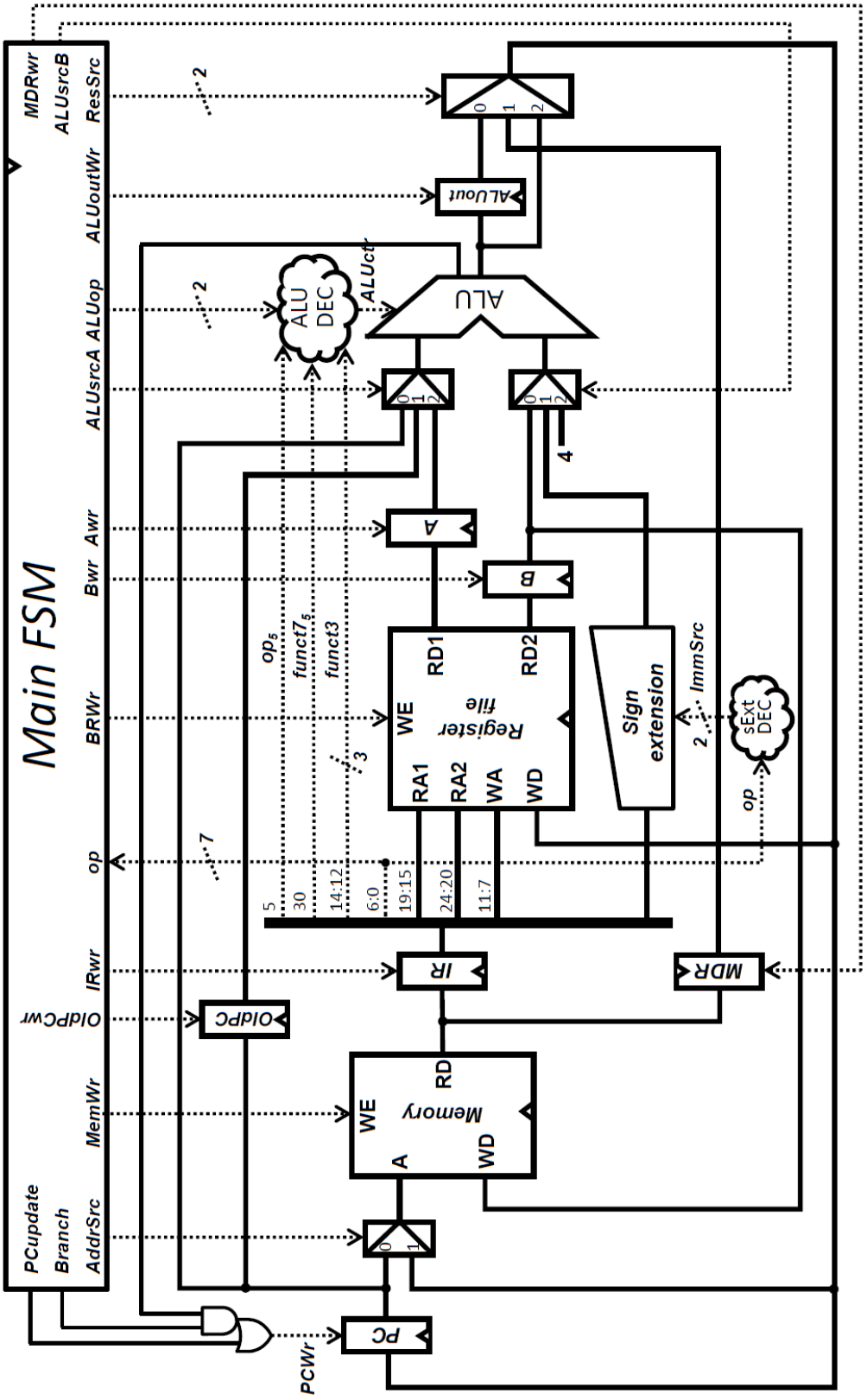
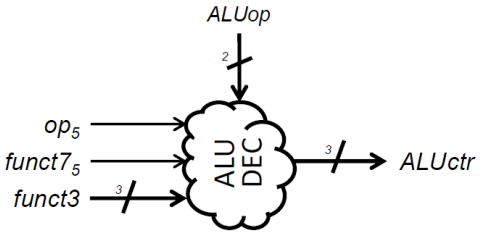
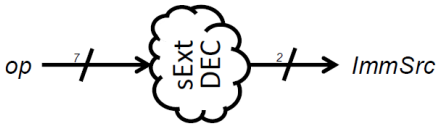
INTRODUCTION TO COMPUTERS II
MULTICYCLE MICROARCHITECTURE

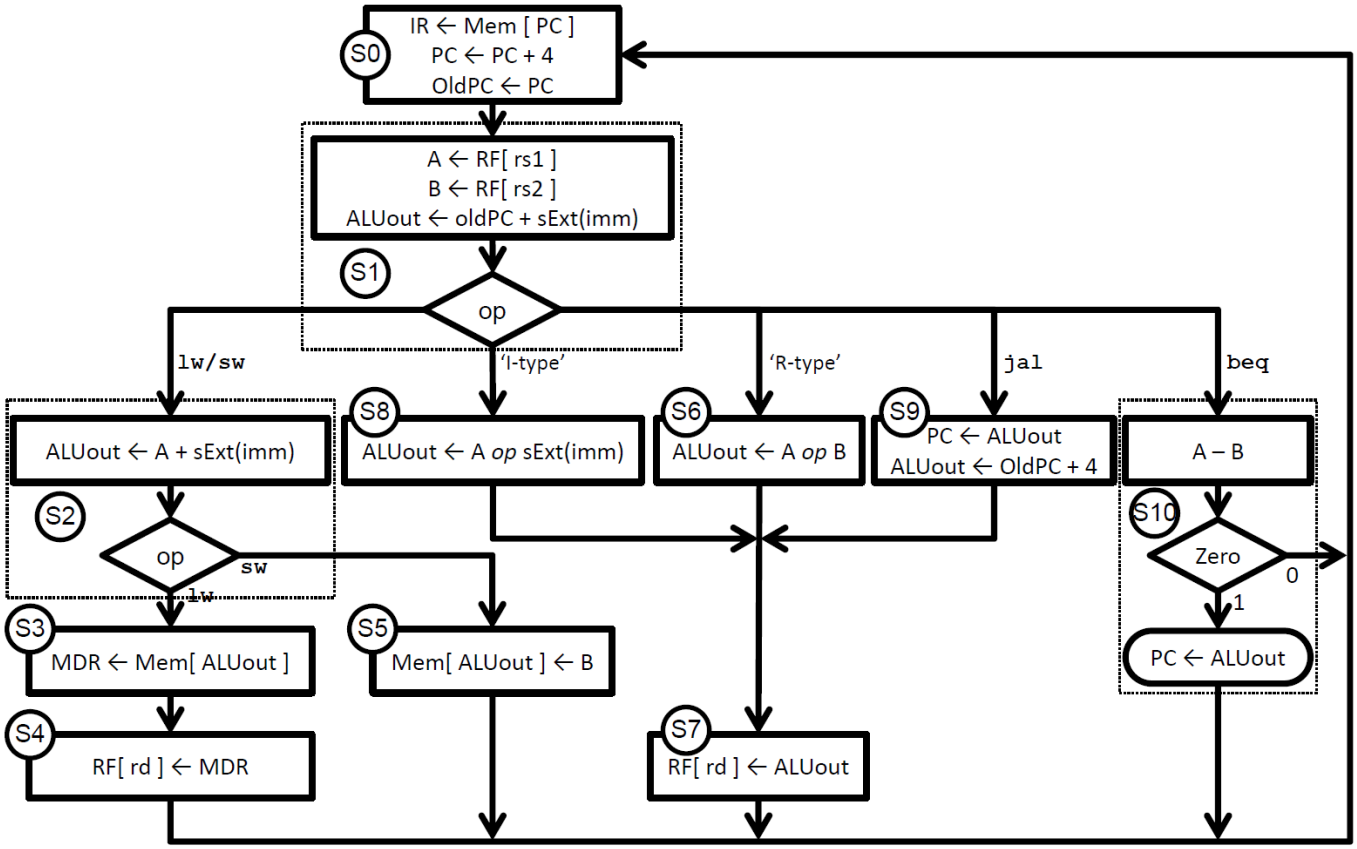


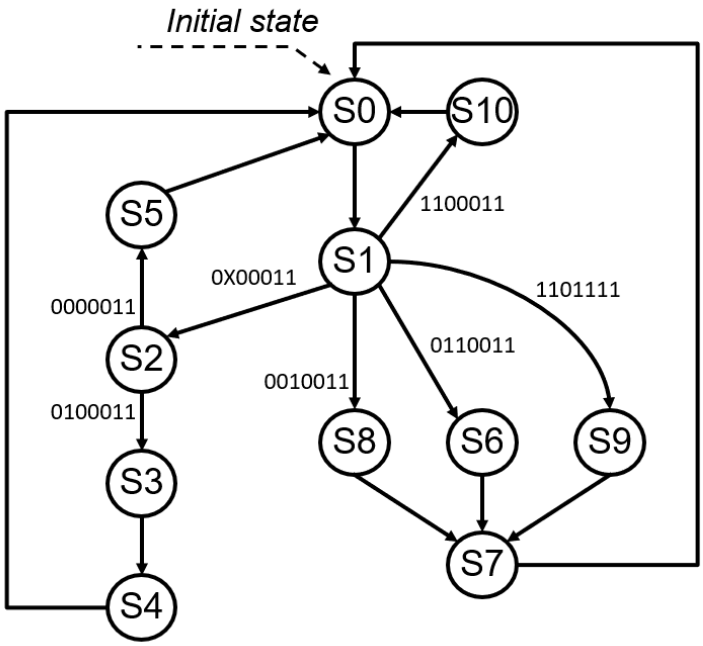


ALUop	op_5	$funct7_5$	funct3	ALUctr
$00^{(add)}$	X	X	XXX	$000^{(A + B)}$
$01^{(subtract)}$	X	X	XXX	$001^{(A - B)}$
$10^{(operate)}$	0	X	$000^{(addi)}$	$000^{(A + B)}$
$10^{(operate)}$	1	0	$000^{(add)}$	$000^{(A + B)}$
$10^{(operate)}$	1	1	$000^{(sub)}$	$001^{(A - B)}$
$10^{(operate)}$	X	X	$010^{(slt/slti)}$	$101^{(A < B)}$
$10^{(operate)}$	X	X	$110^{(or/ori)}$	$011^{(A \mid B)}$
$10^{(operate)}$	X	X	$111^{(and/andi)}$	$010^{(A \& B)}$



Op	ImmSrc
$0000011^{(lw)}$	$00^{(I\text{-type})}$
$0100011^{(sw)}$	$01^{(S\text{-type})}$
$0010011^{(I\text{-type})}$	$00^{(I\text{-type})}$
$0110011^{(R\text{-type})}$	–
$1100011^{(beq)}$	$10^{(B\text{-type})}$
$1101111^{(jal)}$	$11^{(J\text{-type})}$





State transition function

state	op	state'
S0	XXXXXXX	S1
S1	0X00011 (lw/sw)	S2
S1	0010011 (I-type)	S8
S1	0110011 (R-type)	S6
S1	1101111 (jal)	S9
S1	1100011 (beq)	S10
S2	0000011 (lw)	S3
S2	0100011 (sw)	S5
S3	XXXXXXX	S4
S4	XXXXXXX	S0
S5	XXXXXXX	S0
S6	XXXXXXX	S7
S7	XXXXXXX	S0
S8	XXXXXXX	S7
S9	XXXXXXX	S7
S10	XXXXXXX	S0

Output function

state	Branch	PCupdate	AddrSrc	MemWr	OldPCwr	IRwr	MDRwr	BRwr	Awr	Bwr	ALUsrcA	ALUsrcB	ALUop	ALUoutWr	ResSrc
S0	0	1	0	0	1	1	0	0	0	0	00	10	00	0	10
S1	0	0	–	0	0	0	0	0	1	1	01	01	00	1	–
S2	0	0	–	0	0	0	0	0	0	0	10	01	00	1	–
S3	0	0	1	0	0	0	1	0	0	0	–	–	–	0	00
S4	0	0	–	0	0	0	0	1	0	0	–	–	–	0	01
S5	0	0	1	1	0	0	0	0	0	0	–	–	–	0	00
S6	0	0	–	0	0	0	0	0	0	0	10	00	10	1	–
S7	0	0	–	0	0	0	0	1	0	0	–	–	–	0	00
S8	0	0	–	0	0	0	0	0	0	0	10	01	10	1	–
S9	0	1	–	0	0	0	0	0	0	0	01	10	00	1	00
S10	1	0	–	0	0	0	0	0	0	0	10	00	01	0	00