



Module 4 - Problems:

Design of the instruction format

Introduction to Computers II

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1) Given the following RISC-V assembly instructions, provide the corresponding 32-bit machine code.

- a) `lw t0, 0(t2)`
- b) `bge t1, t0, 0x2C`
- c) `sw t1, 0(t4)`

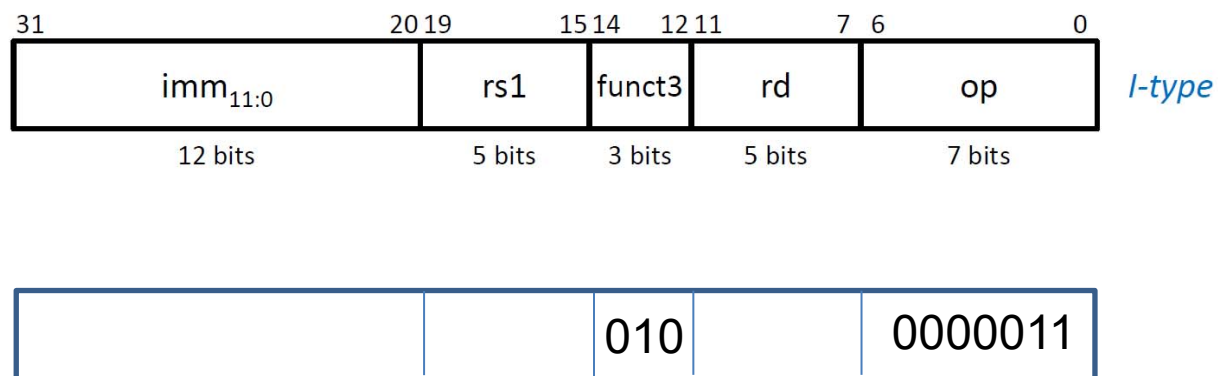
a) `lw t0, 0(t2)` → I-type

Field encoding

Function codes (i)

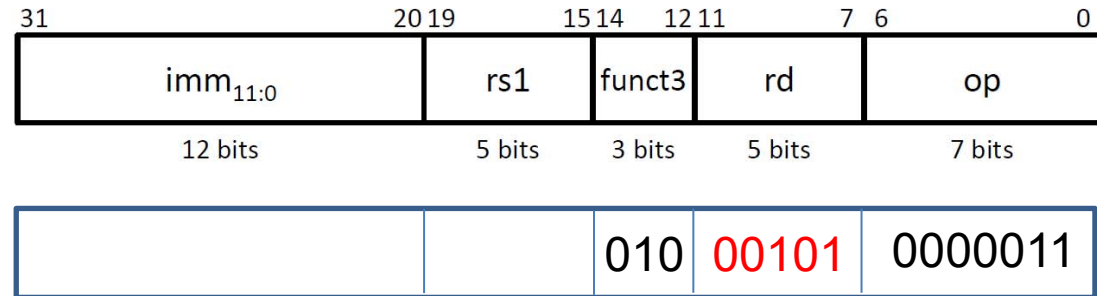
Load instructions

| op | funct3 | Instruction | Type |
|---------|--------|------------------|------|
| | 000 | <code>lb</code> | I |
| | 001 | <code>lh</code> | I |
| 0000011 | 010 | <code>lw</code> | I |
| | 011 | <code>lbu</code> | I |
| | 100 | <code>lhu</code> | I |





a) lw t0, 0(t2) → I-type



Field encoding

Register codes

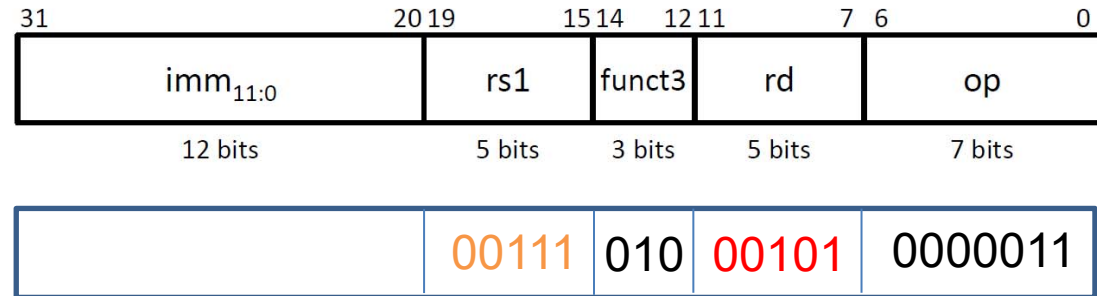
| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
| t2 | x7 | 00111 |
| s0/fp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
| a4 | x14 | 01110 |
| a5 | x15 | 01111 |

| Name | Number | Code |
|------|--------|-------|
| a6 | x16 | 10000 |
| a7 | x17 | 10001 |
| s2 | x18 | 10010 |
| s3 | x19 | 10011 |
| s4 | x20 | 10100 |
| s5 | x21 | 10101 |
| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |





a) lw t0, 0(t2) → I-type



Field encoding

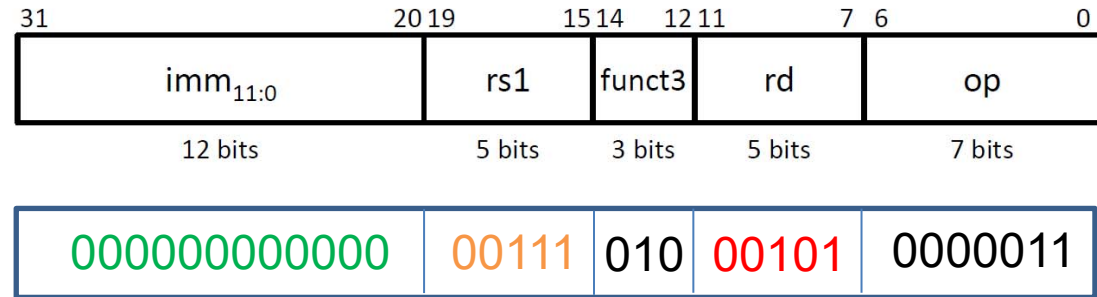
Register codes

| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
| t2 | x7 | 00111 |
| s0/tp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
| a4 | x14 | 01110 |
| a5 | x15 | 01111 |

| Name | Number | Code |
|------|--------|-------|
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| s2 | x18 | 10010 |
| s3 | x19 | 10011 |
| s4 | x20 | 10100 |
| s5 | x21 | 10101 |
| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |



a) lw t0, 0(t2) → I-type



0x0003A283



I-type



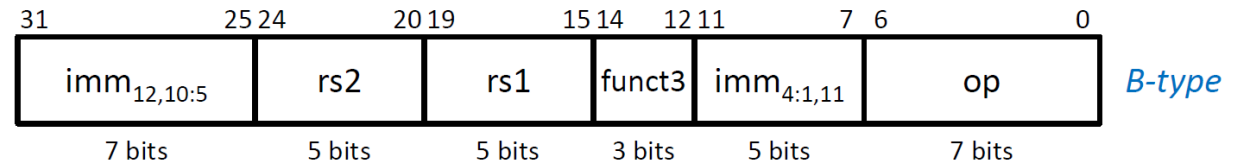
1) Given the following RISC-V assembly instructions, provide the corresponding 32-bit machine code.

a) `lw t0, 0(t2)`

b) `bge t1, t0, 0x2C`

c) `sw t1, 0(t4)`

b) `bge t1,t0,0x2C` → B-type



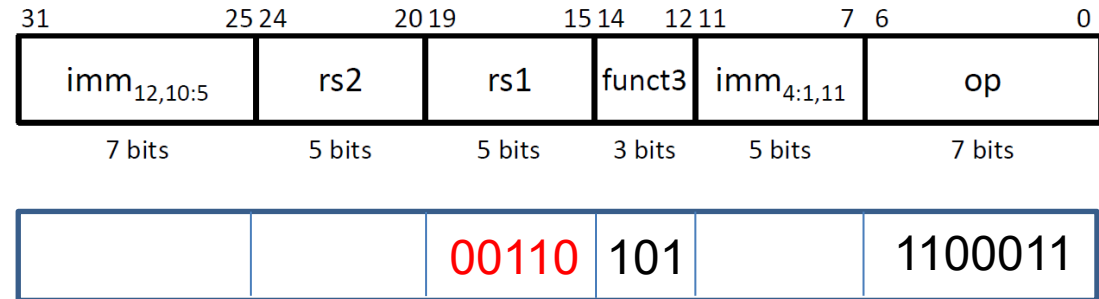
Condition branch instructions

| op | funct3 | Instruction | Type |
|---------|--------|-------------------|------|
| | 000 | <code>beq</code> | B |
| | 001 | <code>bne</code> | B |
| | 100 | <code>blt</code> | B |
| 1100011 | 101 | <code>bge</code> | B |
| | 110 | <code>bltu</code> | B |
| | 111 | <code>bgeu</code> | B |



B-type

b) bge t1,t0,0x2C → B-type



Field encoding

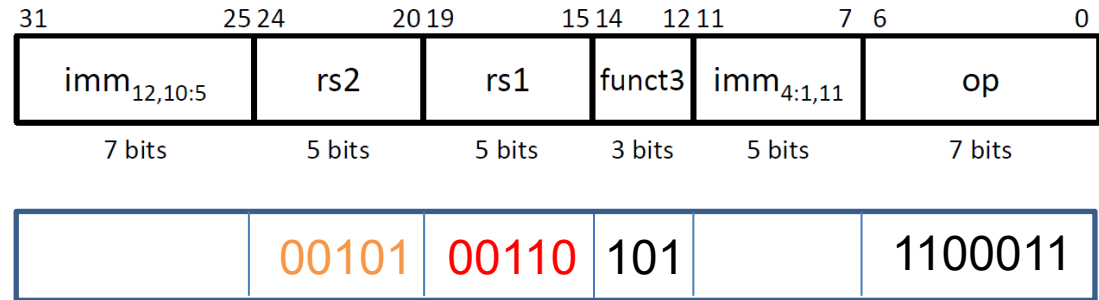
Register codes

| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
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| s0/fp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
| a4 | x14 | 01110 |
| a5 | x15 | 01111 |

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|------|--------|-------|
| a6 | x16 | 10000 |
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| s4 | x20 | 10100 |
| s5 | x21 | 10101 |
| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |



b) bge t1,t0,0x2C → B-type



B-type

Field encoding

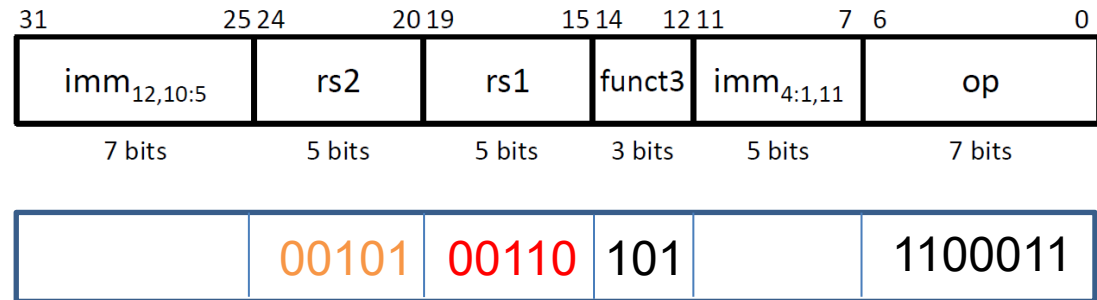
Register codes

| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
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| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
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| t6 | x31 | 11111 |



b) bge t1,t0,0x2C → B-type

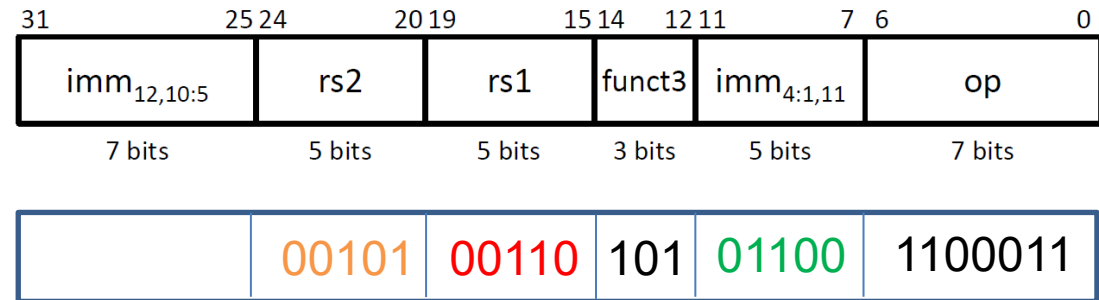


B-type



0x2C → 0b0000000101100

b) bge t1,t0,0x2C → B-type



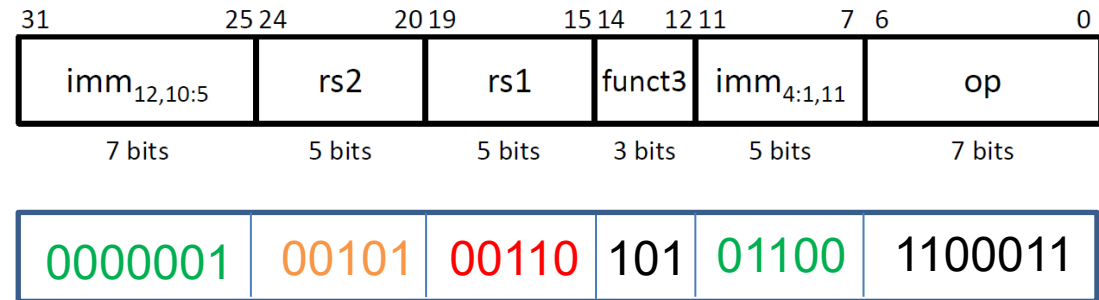
B-type



0x2C → 0b000000101100

b) bge t1,t0,0x2C → B-type

0x2C → 0b000000101100



B-type



0x02535663



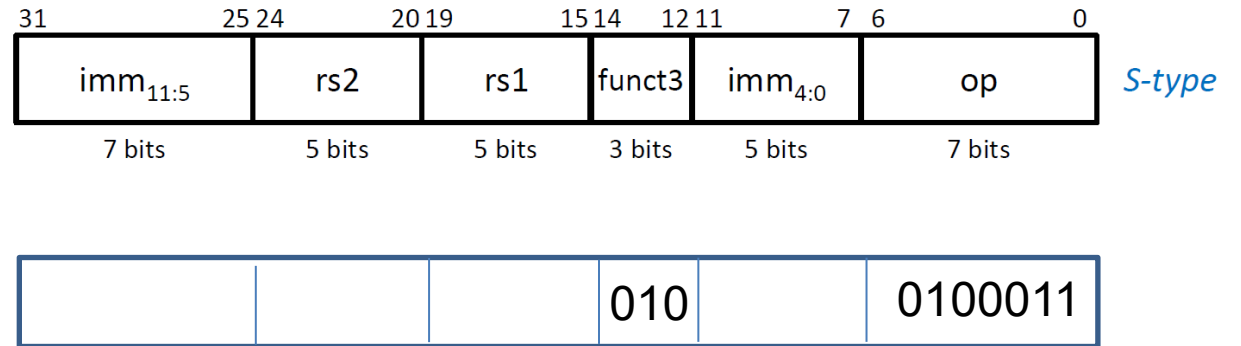
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c) `sw t1, 0(t4)` → S-type

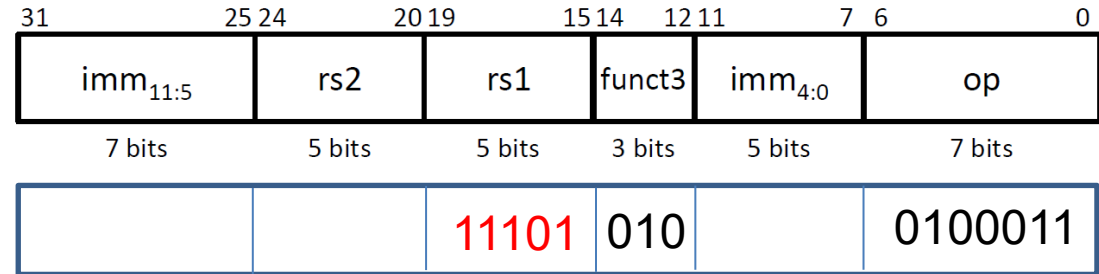


Store instructions

| op | funct3 | Instruction | Type |
|---------|--------|-----------------|------|
| | 000 | <code>sb</code> | S |
| 0100011 | 001 | <code>sh</code> | S |
| | 010 | <code>sw</code> | S |



c) `sw t1, 0(t4)` → S-type



Field encoding

Register codes

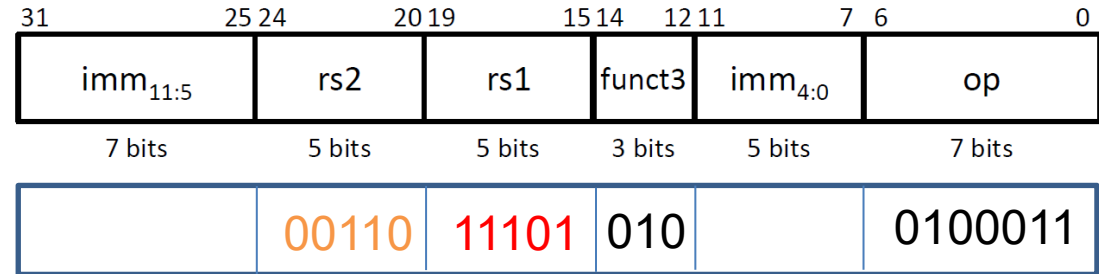
| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
| t2 | x7 | 00111 |
| s0/fp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
| a4 | x14 | 01110 |
| a5 | x15 | 01111 |

| Name | Number | Code |
|------|--------|-------|
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| a7 | x17 | 10001 |
| s2 | x18 | 10010 |
| s3 | x19 | 10011 |
| s4 | x20 | 10100 |
| s5 | x21 | 10101 |
| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |





c) sw t1, 0(t4) → S-type



Field encoding

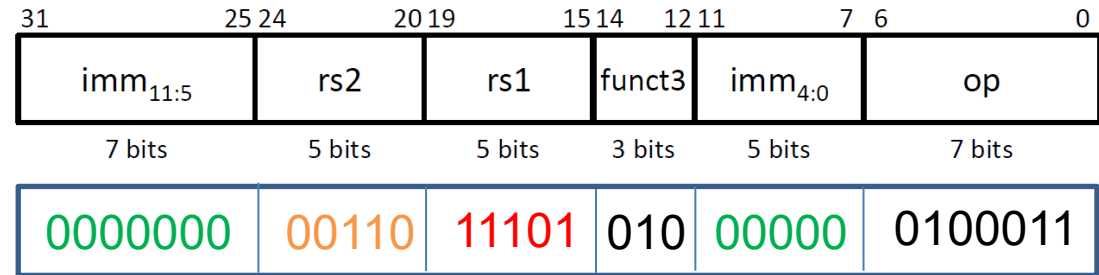
Register codes

| Name | Number | Code |
|-----------|-----------|--------------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
| t2 | x7 | 00111 |
| s0/fp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
| a4 | x14 | 01110 |
| a5 | x15 | 01111 |

| Name | Number | Code |
|------|--------|-------|
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| a7 | x17 | 10001 |
| s2 | x18 | 10010 |
| s3 | x19 | 10011 |
| s4 | x20 | 10100 |
| s5 | x21 | 10101 |
| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |



c) sw t1, 0(t4) → S-type



0x006EA023



S-type



2) Given the following RISC-V 32-bit machine code, provide the corresponding assembly instructions.

- a) 0x03528b33
- b) 0x00190913
- c) 0x0000006F

a) 0x03528B33

00000011010100101000101100110011



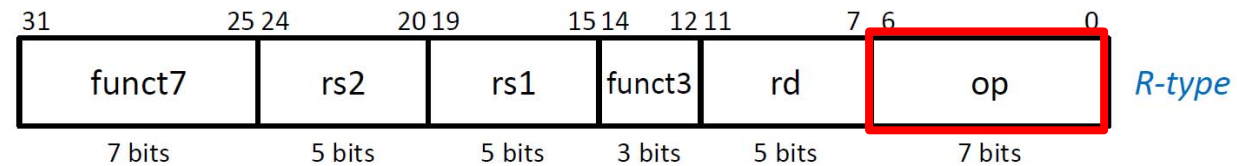
2) Given the following RISC-V 32-bit machine code, provide the corresponding assembly instructions.

- a) 0x03528b33
- b) 0x00190913
- c) 0x0000006F

a) 0x03528B33

00000011010100101000101100110011

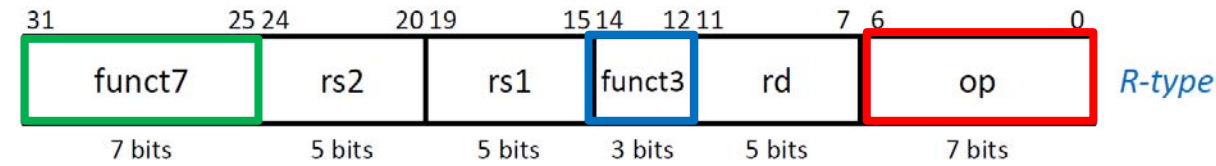
| op | Instruction | Type |
|---------|---|------|
| 0000011 | load | I |
| 0010011 | arithmetic-logic and shift with immediate operand | I |
| 0010111 | auipc | U |
| 0100011 | store | S |
| 0110011 | arithmetic-logic and shift with register operands | R |
| 0110111 | lui | U |
| 1100011 | branch | B |
| 1100111 | jalr | I |
| 1101111 | jal | J |





a) 0x03528B33

00000011010100101000101100110011



Multiplication and division instructions*

| op | funct3 | funct7 | Instruction | Type |
|---------|--------|---------|-------------|------|
| | 000 | 0000001 | mul | R |
| | 001 | 0000001 | mulh | R |
| | 010 | 0000001 | mulhsu | R |
| | 011 | 0000001 | mulhu | R |
| 0110011 | 100 | 0000001 | div | R |
| | 101 | 0000001 | divu | R |
| | 110 | 0000001 | rem | R |
| | 111 | 0000001 | remu | R |

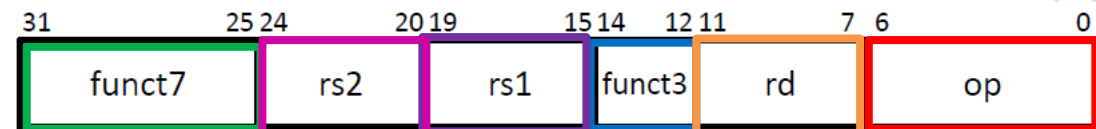
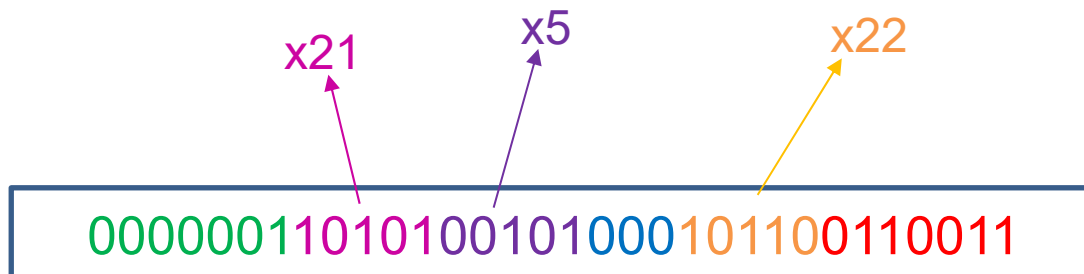


mul instruction

*Defined in the RVM extension



a) 0x03528B33



tipo-R

Field encoding

Register codes

| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
| t2 | x7 | 00111 |
| s0/fp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
| a4 | x14 | 01110 |
| a5 | x15 | 01111 |

| Name | Number | Code |
|------|--------|-------|
| a6 | x16 | 10000 |
| a7 | x17 | 10001 |
| s2 | x18 | 10010 |
| s3 | x19 | 10011 |
| s4 | x20 | 10100 |
| s5 | x21 | 10101 |
| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |



mul s6,t0,s5



2) Given the following RISC-V 32-bit machine code, provide the corresponding assembly instructions.

- a) 0x03528b33
- b) 0x00190913
- c) 0x0000006F

b) 0x00190913

00000000000110010000100100010011



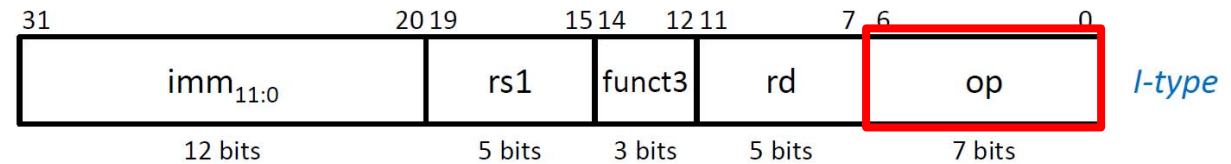
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- a) 0x03528b33
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- c) 0x0000006F

b) 0x00190913

00000000000110010000100100010011

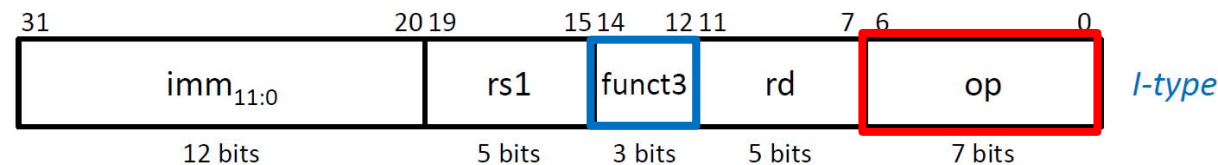
| op | Instruction | Type |
|---------|---|------|
| 0000011 | load | I |
| 0010011 | arithmetic-logic and shift with immediate operand | I |
| 0010111 | auipc | U |
| 0100011 | store | S |
| 0110011 | arithmetic-logic and shift with register operands | R |
| 0110111 | lui | U |
| 1100011 | branch | B |
| 1100111 | jalr | I |
| 1101111 | jal | J |





b) 0x00190913

000000000000110010000100100010011



Arithmetic-logic and shift instructions with immediate operand

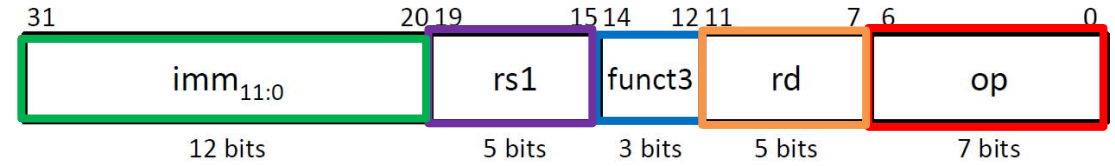
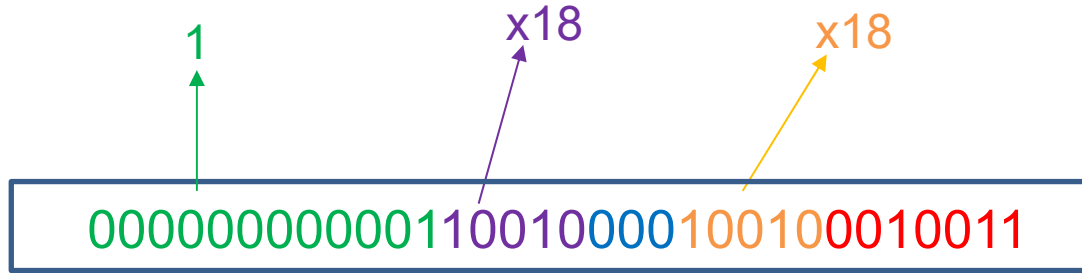
| op | funct3 | funct7* | Instruction | Type |
|---------|--------|----------|-------------|------|
| | 000 | - | addi | |
| | 001 | 0000000* | slli | |
| | 010 | - | slti | |
| | 011 | - | sltiu | |
| 0010011 | 100 | - | xori | |
| | 101 | 0000000* | srlr | |
| | 101 | 0100000* | srai | |
| | 110 | - | ori | |
| | 111 | - | andi | |



addi instruction



b) 0x00190913



I-type

Field encoding

Register codes

| Name | Number | Code |
|-------|--------|-------|
| zero | x0 | 00000 |
| ra | x1 | 00001 |
| sp | x2 | 00010 |
| gp | x3 | 00011 |
| tp | x4 | 00100 |
| t0 | x5 | 00101 |
| t1 | x6 | 00110 |
| t2 | x7 | 00111 |
| s0/fp | x8 | 01000 |
| s1 | x9 | 01001 |
| a0 | x10 | 01010 |
| a1 | x11 | 01011 |
| a2 | x12 | 01100 |
| a3 | x13 | 01101 |
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| a5 | x15 | 01111 |

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|------|--------|-------|
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| s6 | x22 | 10110 |
| s7 | x23 | 10111 |
| s8 | x24 | 11000 |
| s9 | x25 | 11001 |
| s10 | x26 | 11010 |
| s11 | x27 | 11011 |
| t3 | x28 | 11100 |
| t4 | x29 | 11101 |
| t5 | x30 | 11110 |
| t6 | x31 | 11111 |



addi s2,s2,1



2) Given the following RISC-V 32-bit machine code, provide the corresponding assembly instructions.

- a) 0x03528b33
- b) 0x00190913
- c) 0x0000006F

c) 0x0000006F

000000000000000000000000000000001101111



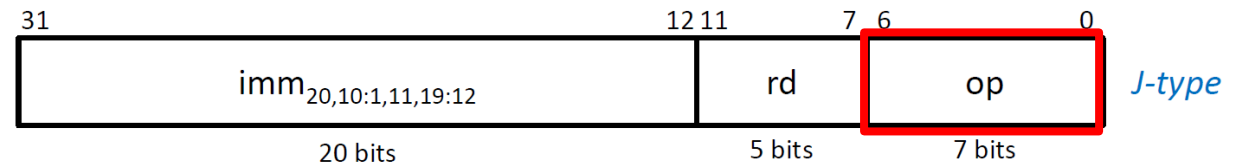
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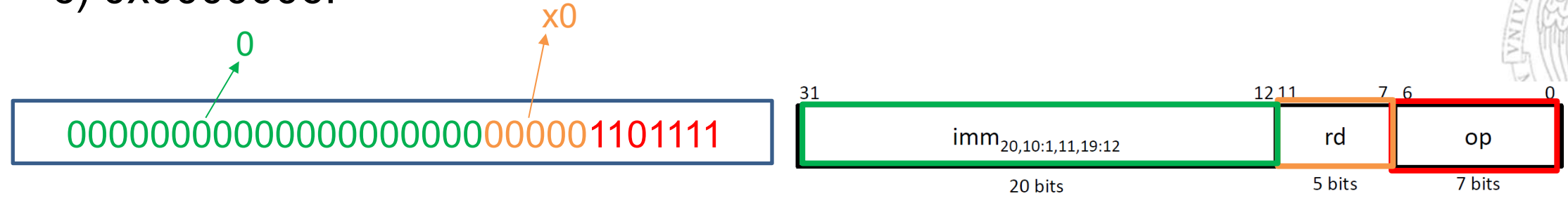
| op | Instruction | Type |
|---------|---|------|
| 0000011 | load | I |
| 0010011 | arithmetic-logic and shift with immediate operand | I |
| 0010111 | auipc | U |
| 0100011 | store | S |
| 0110011 | arithmetic-logic and shift with register operands | R |
| 0110111 | lui | U |
| 1100011 | branch | B |
| 1100111 | jalr | I |
| 1101111 | jal | J |





J-type

c) 0x0000006F



jal x0,0



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