Facultad de Informática
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INTRODUCTION TO COMPUTERS II
MODULE 4

Basic problems:

1. Given the following RISC-V assembly instructions, provide the corresponding 32-bit machine code.

a) **`lw t0, 0(t2)`** b) **`bge t1, t0, 0x2C`** c) **`sw t1, 0(t4)`**

2. Given the following RISC-V 32-bit machine code, provide the corresponding assembly instructions.

a) `0x03528b33` b) `0x00190913` c) `0x0000006f`

Additional problems:

3. Suppose that a new instruction is added to the RISC-V ISA. This instruction reads a word from memory using a base register and a variable offset stored in an index register, **`lwi rd, rs1, rs2`**:

{ rd ← Mem[rs1+ rs2] }

Provide:

a) The most appropriate format, among the existing ones, to encode this instruction.
b) The smallest RISC-V instruction sequence needed to implement it as a pseudo-instruction.

4. Suppose that a new instruction is added to the RISC-V ISA. This instruction loads a word from memory, pre-incrementing the base register, **`lwpreinc rd, imm(rs1)`**:

{ rd ← Mem[rs1 + sExt(imm)], rs1 ← rs1 + sExt(imm) }

Provide:

a) The most appropriate format, among the existing ones, to encode this instruction.
b) The smallest RISC-V instruction sequence needed to implement it as a pseudo-instruction.

5. Suppose that a new instruction is added to the RISC-V ISA. This instruction loads a word from memory, post-incrementing the base register, **`lwpostinc rd, imm(rs1)`**:

{ rd ← Mem[rs1], rs1 ← rs1 + sExt(imm) }

Provide:

a) The most appropriate format, among the existing ones, to encode this instruction.
b) The smallest RISC-V instruction sequence needed to implement it as a pseudo-instruction.

6. Suppose that a new instruction is added to the RISC-V ISA. This instruction swaps the value of 2 registers, **`swap rs1, rs2`**:

{ rs1 ← rs2, rs2 ← rs1}

Provide:

a) The most appropriate format, among the existing ones, to encode this instruction.
b) The smallest RISC-V instruction sequence needed to implement it as a pseudo-instruction.

7. Suppose that a new instruction is added to the RISC-V ISA. This instruction loads a data read from a certain memory position into a register, **`lwa`** ***`rd, imm`***:

{ rd ← Mem[zExt(imm)] }

Provide:

a) The most appropriate format, among the existing ones, to encode this instruction.
b) The smallest RISC-V instruction sequence needed to implement it as a pseudo-instruction.

8. Provide the RISC-V machine code for each of the following assembly instructions:

a) `sub  x5, x6, x7`
b) `addi s0, s1, 12`
c) `lw   t2, -6(s3)`
d) `srai t1, t2, 29`
e) `sb t5, 45(zero)`
f) `beq s0, t5, 0x10`
g) `lui s5, 0x8cdef`
h) `jal ra, 0xa67f8`

9. Provide the RISC-V assembly instructions for each of the following machine codes:

a) `0x41fe83b3`
b) `0xfda48293`
c) `0x05ce2a03`