INTRODUCTION TO COMPUTERS II

MODULE 6

Basic problems:

1. Provide the value of the control signals produced in a multicycle RISC-V when executing a **`sw`** instruction.
2. Provide the value of the control signals produced in a multicycle RISC-V when executing an **`add`** instruction.
3. Provide the value of the control signals produced in a multicycle RISC-V when executing a **`jal`** instruction.
4. A given program, which is running on a multicycle processor, needs an average of 4.25 cycles per instruction. The program is formed by 10,000 instructions, with the following distribution: 30% are **`lw`**, 15% are **`sw`**, 20% are arithmetic-logic and the rest are **`jal`** and **`beq`**. Determine how many **`jal`** instructions and how many **`beq`** instructions are in such program.
5. A certain multicycle processor is running a program with 140 instructions. 70 of these instructions take 4 cycles to execute, 35 take 5 cycles, 20 take 3 cycles and the other 15 take 7 cycles. Calculate the CPI of this program. If the processor works with a 2 GHz frequency, calculate the execution time of the program.
6. Consider two multicycle processors with the following features:
   - PowerPC, which works with a 1.8 GHz frequency and 700 MIPS.
   - Pentium 4, which works with a 1.6 GHz frequency and 850 MIPS.

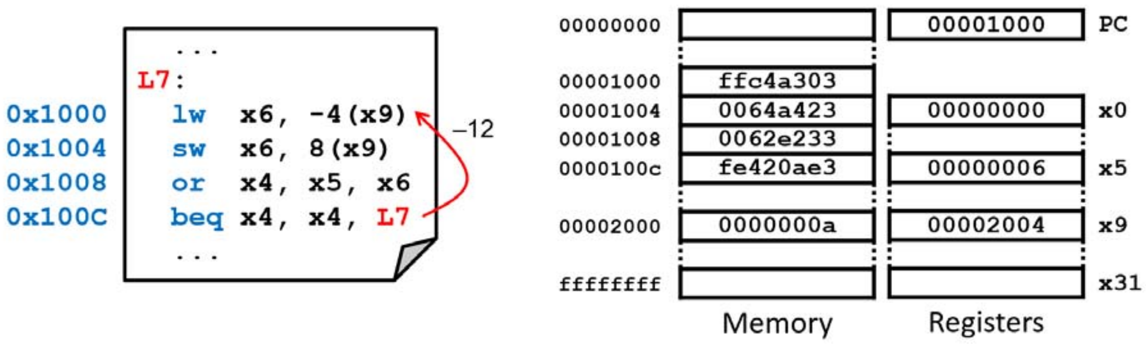
   Calculate the CPI of each processor.
7. Consider the two processors of the previous exercise. When running a certain program, the processors obtain a CPI of 5.5 (PowerPC) and 7 (Pentium 4). The machine code generated by the compiler has 9 million instructions (PowerPC) and 7.2 million instructions (Pentium). Which computer will run the program faster?
8. A given program runs on two multicycle processors (A and B), which work with 1 GHz and 1.5 GHz frequencies, respectively. The distribution of the program instructions running on A is as follows:

	arithmetic	load	store	branch
frequency	50%	25%	10%	15%
cycles	4	5	4	3

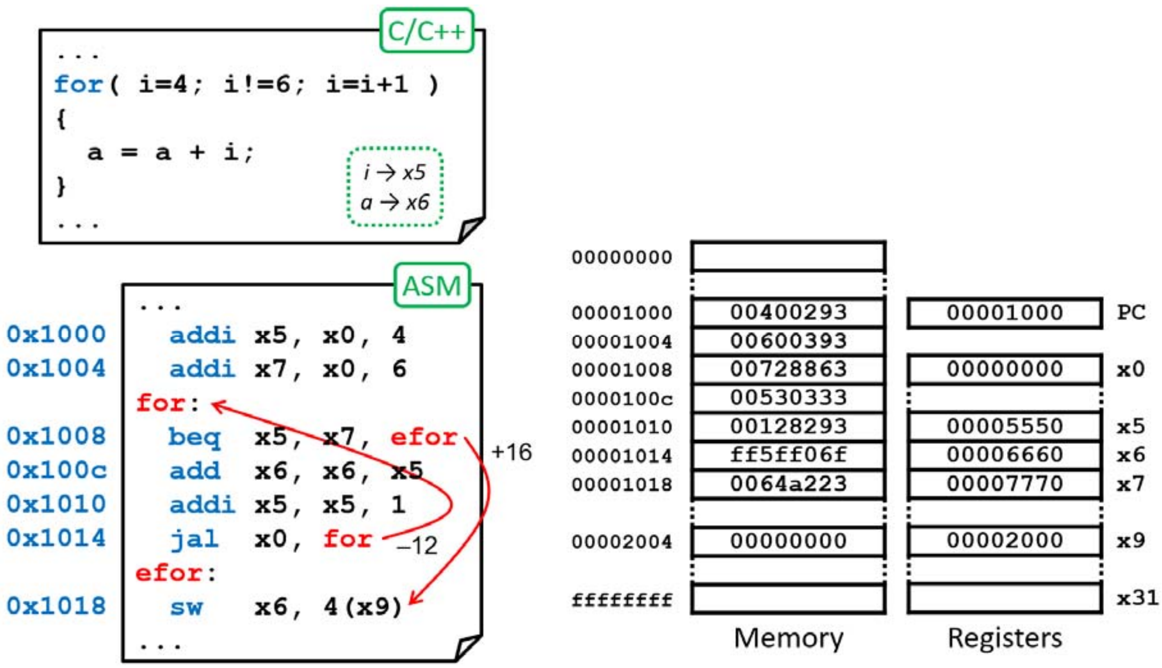
   a) Calculate the CPI of the program running on processor A.
   b) The number of instructions running on B is 60% of the executed in A, and its execution time is half the time in A. Calculate the CPI of the program running on processor B.

Additional problems:

9. Assume that the following program is running on a multicycle RISC-V, with the initial value of the memory and registers shown in the picture. Represent the execution diagrams for the registers and the memory, as well as for the control and status signals, so that their values are shown for each clock cycle.



10. Assume that the following program is running on a multicycle RISC-V, with the initial value of the memory and registers shown in the picture. Represent the execution diagrams for the registers and the memory, as well as for the control and status signals, so that their values are shown for each clock cycle.



11. When silicon chips are fabricated, defects in materials and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get damaged and always register a logical 0 (stuck-at-0) or a logical 1 (stuck-at-1). Indicate what multicycle RISC-V instructions would fail if the following control signals suffered a stuck-at-0 defect:

a) $ResSrc_0$
b) $ALUsrcB_1$
c) $ALUsrcB_0$
d) $ALUsrcA_1$
e) $ALUsrcA_0$
f) $ImmSrc_1$
g) $ImmSrc_0$
h) PCupdate
i) Branch
j) AddrSrc
k) MemWr
l) IRwr

12. Repeat the previous exercise, but now with a stuck-at-1 defect.

13. Discuss the modifications required in the data path and the controller ASM diagram of the multicycle RISC-V, in order to extend its ISA with each of the following instructions:

a) **`xor`** / **`xori`**
b) **`sll`** / **`ssli`**
c) **`bne`** / **`blt`** / **`bge`**
d) **`slt`** / **`slti`**
e) **`lb`** / **`lh`** / **`lbu`** / **`lhu`**
f) **`sb`** / **`sh`**
g) **`jarl`**
h) **`lui`**
i) **`auipc`**

14. Discuss the modifications required in the data path and the controller ASM diagram of the multicycle RISC-V, in order to extend its ISA with a new I-type instruction that reads a word from memory, pre-incrementing the base register, **`lwpreinc`** ***`rd, imm(rs1)`***:

{ rd ← Mem[rs1 + sExt(imm)], rs1 ← rs1 + sExt(imm) }

15. Discuss the modifications required in the data path and the controller ASM diagram of the multicycle RISC-V, in order to extend its ISA with a new I-type instruction that reads a word from memory, post-incrementing the base register, **`lwpostinc`** ***`rd, imm(rs1)`***:

{ rd ← Mem[rs1], rs1 ← rs1 + sExt(imm) }

16. Discuss the modifications required in the data path and the controller ASM diagram of the multicycle RISC-V, in order to extend its ISA with a new I-type instruction that stores the result of an immediate addition in memory, **`swaddi`** ***`rs1, rs2, imm`***:

{ Mem[rs1] ← rs2 + sExt(imm) }

17. Discuss the modifications required in the data path and the controller ASM diagram of the multicycle RISC-V, in order to extend its ISA with a new I-type instruction that adds a register with a data read from memory, **`addm`** ***`rd, rs1, imm`***:

{ rd ← rd + Mem[rs1 + sExt(imm)] }

18. Discuss the modifications required in the data path and the controller ASM diagram of the multicycle RISC-V, in the case the register file had a unique read port, instead of two. How many cycles would be required to execute each instruction? Would the processor cycle time be reduced? And in the case the register file had a unique read/write port?

19. Suppose that the register file of the multicycle processor could be redesigned so that it requires half the area, but at the expense of doubling its access delays. Would this change make sense?

20. If you could reduce the delay of just one of the components of the multicycle RISC-V in the 90nm CMOS library by half, which one would you choose to get a smaller cycle time? What would be the value of the new cycle time?

21. If the ALU delay is reduced a 30%, the extension sign module delay a 10% and the register file read/write delays a 20% (referred to the multicycle RISC-V with the 90nm CMOS library), calculate:

a) The delay of the critical path for each state.
b) The speed-up obtained when running a program with 100 million instructions.

22. Assuming that the instructions of a certain program running on a multicycle RISC-V follow this distribution:

	arithmetic	load/store	branch
frequency	60%	25%	15%
cycles	4	6	3

a) Calculate the CPI.
b) If we want to improve its performance a 25%, how many cycles (on average) would an optimized arithmetic instruction take to execute, if the rest of the instructions are not modified?
c) Same if we want to improve its performance a 50%.

23. Suppose that a new arithmetic instruction is added to the multicycle RISC-V ISA, which reduces the number of executed arithmetic instructions in 25%, but increases the cycle time a 10%. Does this change make sense?

	arithmetic	load/store	branch
frequency	60%	25%	15%
cycles	4	6	3

Exam problems:

24. (Adapted September 2016) The program fragment shown below is running on a multicycle RISC-V, which has a 1 GHz frequency, producing an execution time of 3,474 ns.

```
        mv   s4, zero
        la   s5, A
        mv   s6, zero
        li   s4, 127
L1:     slli s3, s4, 2
        add  s3, s3, s5
        lw   s0, 0(s3)
        add  s6, s6, s0
        add  s4, s4, -1
        bge  s4, zero, L1
L2:
    ... (rest of the program)
```

a) Calculate the CPI of this program fragment.
b) Calculate the value of the MIPS metric.