Facultad de Informática
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INTRODUCTION TO COMPUTERS II
MODULE 8

Basic problems:

1. Indicate the code loaded in **`mcause`** if the execution of the following instructions produces an exception in a full RISC-V processor without RVM extension:

a) **`lb`**	b) **`addi`**	c) **`slt`**	d) **`lw`**
e) **`mul`**	f) **`jalr`**	g) **`sw`**	h) **`lui`**
f) **`ecall`**	g) **`csrw`**	h) **`mret`**	i) **`auipc`**

2. Repeat the previous exercise assuming that the instructions are now executed on the reduced architecture RISC-V.

3. Consider a processor on cycle 100 of the execution of a certain program. In that cycle, depending on the case, the MIErr/MDErr/MErr signal is activated. Indicate on which cycle the ESR would start executing, assuming that the microarchitecture is:
a) Single-cycle b) Multicycle c) Pipelined

4. Repeat the previous exercise assuming that the OpErr signal is now activated.

5. Consider a processor that, at cycle 100, begins executing an instruction that will generate a memory access exception. That is, depending on the case, the MIErr/MDErr/MErr signal will be activated at the corresponding cycle. Indicate on which cycle the ESR would start executing, assuming that the microarchitecture is:
a) Single-cycle b) Multicycle c) Pipelined

6. Repeat the previous exercise assuming that the OpErr signal is now activated.

7. Justify if the execution of the same instruction can produce the activation of several exception signals in the same cycle, for each of the following microarchitectures:
a) Single-cycle b) Multicycle c) Pipelined

Additional problems:

8. Discuss the modifications to the data path of the reduced architecture RISC-V required to extend its ISA with the **`ecall`** instruction.
a) Single-cycle b) Multicycle c) Pipelined

Exam problems:

9. (May 2024, adapted) Suppose that instruction **`lw s1,0(t1)`** triggers an exception in the pipelined processor. Indicate:
a) What type of exception would it be?
b) In what stage of the processor would it occur?
c) In what cycle would it happen?
d) What specific circumstance has happened for this exception to occur and why?
e) What fetched instructions would be cancelled?

8. (June 2024, adapted) Assuming the reduced architecture pipelined RISC-V, answer the following questions:

a) Could the `sb t2,0(t0)` instruction produce a misaligned address exception?
b) The `xor t2,t2,s2` instruction produces an exception when executed. What kind would it be?
c) In what cycle and stage of the processor would the exception from the previous question first occur?
d) In what cycle would the ESR start executing after the previous exception occurs?

Solutions

1. a) none b) none c) none d) 4
e) 2 f) 0 g) 6 h) none
f) 11 g) none h) 0 i) none

2. a) 2 b) none c) none d) 4
e) 2 f) 2 g) 6 h) 2
f) 2 g) none h) 0 i) 2

3. a) 101 b) 102 c) 101 ó 104

4. a) 101 b) 102 c) 103

5. a) 101 b) 102 ó 105 c) 104

6. a) 101 b) 103 c) 104

7. a) Yes b) No c) No

8. a) Add a combinational block to activate a new control signal, isEcall, when the execution of `ecall` is detected.
Connect that signal to the OR gate that controls the load of the mcause register.
Modify the encoder of mcause to generate the 0x000b value when the previous signal is activated.
b) Add a combinational block to activate a new control signal, isEcall, when the execution of `ecall` is detected.
Add a transition from S1 to SE when isEcall is 1.
c) Same as in the single-cycle, but delaying the isEcall signal through the IF/ID, ID/EX and EX/MEM pipeline registers.

9. a) Misaligned access to the data memory
b) MEM stage, cycle 5 c) Data in **t1** is not a multiple of 4.
d) That instruction and the 3 following ones.

10. a) No b) Illegal instruction c) EX stage, cycle 10 d) Cycle 12