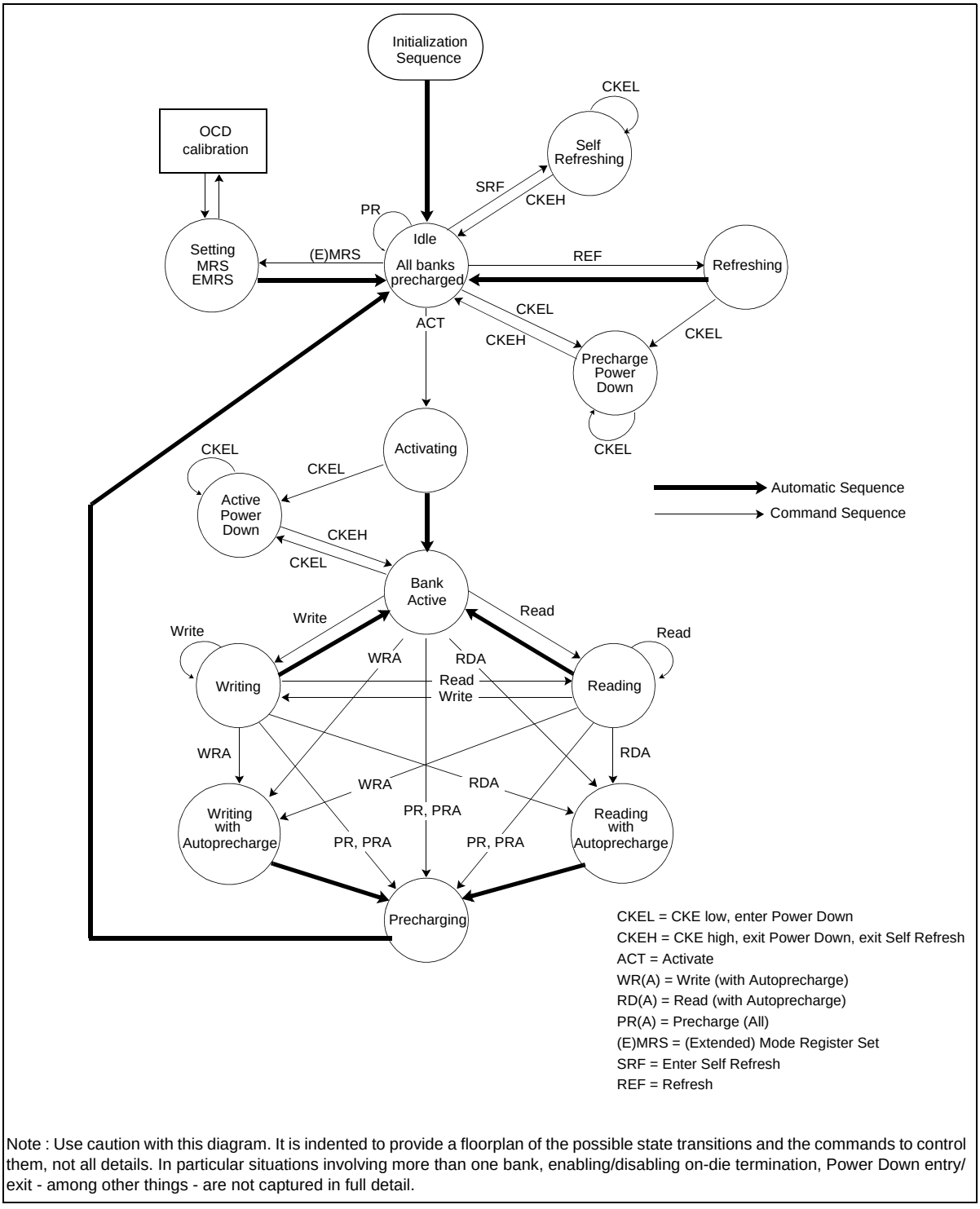
# DDR2 SDRAM

# Device Operating & Timing Diagram

# Functional Description

## Simplified State Diagram




Note : Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit - among other things - are not captured in full detail.

## Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

## Power up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

**Power-up and Initialization Sequence**

1. The following sequence is required for POWER UP and Initialization.
   Apply power and attempt to maintain CKE below 0.2*$V_{DDQ}$ and ODT[*1] at a low state (all other inputs may be undefined.) The power voltage ramps are without any slope reversal, ramp time must be no greater than 200mS; and during the ramp, $V_{DD}$>$V_{DDL}$>$V_{DDQ}$ and $V_{DD}$-$V_{DDQ}$<0.3 volts.

- $V_{DD}$[*2], $V_{DDL}$[*2] and $V_{DDQ}$ are driven from a single power converter output, AND
- $V_{TT}$ is limited to 0.95 V max, AND
- Vref tracks $V_{DDQ}$/2.

or

- Apply $V_{DD}$[*2] before or at the same time as $V_{DDL}$.
- Apply $V_{DDL}$[*2] before or at the same time as $V_{DDQ}$.
- Apply $V_{DDQ}$ before or at the same time as $V_{TT}$ & $V_{REF}$.

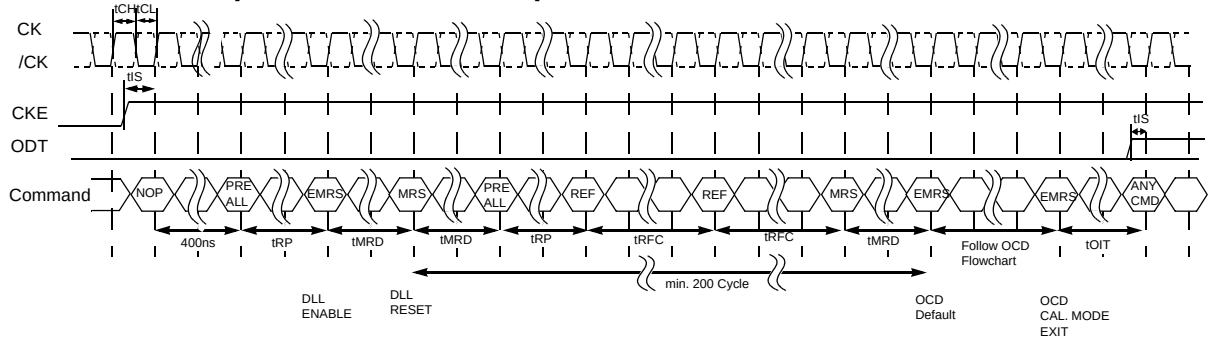
at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200μs after stable power and clock(CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “Low” to BA0, “High” to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “High” to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-2 and A13-A15.)
8. Issue a Mode Register Set command for “DLL reset”[*2].
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-1)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL)
12. At least 200 clocks after step 8, execute OCD Calibration ( Off Chip Driver impedance adjustment ).
    If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

*1) To guarantee ODT off, $V_{REF}$ must be valid and a low level must be applied to the ODT pin.

*2) If DC voltage level of $V_{DDL}$ or $V_{DD}$ is intentionally changed during normal operation, (for example, for the purpose of $V_{DD}$ corner test, or power saving) “DLL Reset” must be executed.

## Initialization Sequence after Power Up



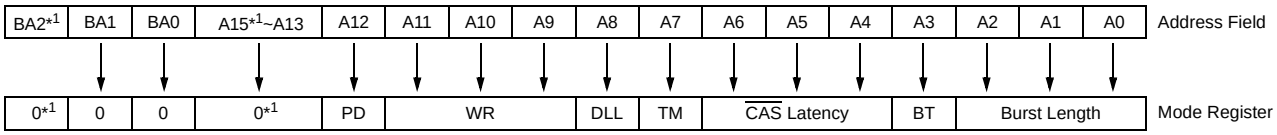

## Programming the Mode and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{CAS}$ latency, DLL reset function, write recovery time(WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT(On Die Termination), single-ended strobe, and OCD(off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register(MR) or Extended Mode Registers(EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

## DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{CAS}$ latency, burst length, burst sequence, test mode, DLL reset, WR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, $\overline{CAS}$ latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time WR is defined by A9 ~ A11. Refer to the table for specific codes.




| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| A7 | mode |
|---|---|
| 0 | Normal |
| 1 | Test |

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

**Burst Length**

| A2 | A1 | A0 | BL |
|---|---|---|---|
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |

| A12 | Active power down exit time |
|---|---|
| 0 | Fast exit(use tXARD) |
| 1 | Slow exit(use tXARDS) |

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2): Reserved |
| 1 | 1 | EMRS(3): Reserved |

**Write recovery for autoprecharge**

| A11 | A10 | A9 | WR(cycles) |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

*2

DDR2-400
DDR2-533
DDR2-667
DDR2-800

**$\overline{CAS}$ Latency**

| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 (Optional) |
| 0 | 1 | 1 | 3 (speed bin determined)* |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 (speed bin determined)* |
| 1 | 1 | 0 | 6 (speed bin determined)* |
| 1 | 1 | 1 | Reserved |

* speed bin determined
= Not required on all speed bin

*1 : A13 is reserved for future use and must be programmed to 0 when setting the mode register.
BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

*2 : WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up a non-integer value to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

# DDR2 SDRAM Extended Mode Register Set

## EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0, while controlling the states of address pins A0 ~ A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Extended Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength data-output driver. A3~A5 determines the additive latency, A2 and A6 are used for ODT value selection, A7~A9 are used for OCD control, A10 is used for DQS# disable and A11 is used for RDQS enable.

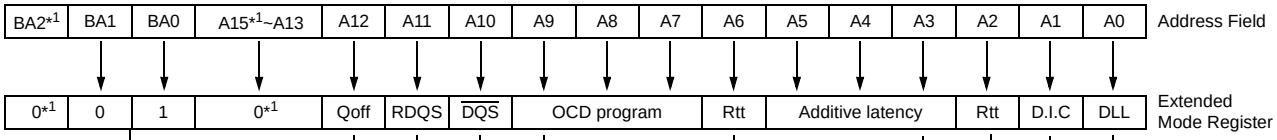
## DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

## EMRS(2)

The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be written after power-up for proper operation. The extended mode register(2) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and low on BA0, while controlling the ststes of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

## EMRS(1) Programming




| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2) |
| 1 | 1 | EMRS(3): Reserved |

| A6 | A2 | Rtt (NOMINAL) |
|---|---|---|
| 0 | 0 | ODT Disabled |
| 0 | 1 | 75 ohm |
| 1 | 0 | 150 ohm |
| 1 | 1 | 50 ohm[a] |

a : Optional for DDR2-400/533/667

| A0 | DLL Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A1 | Output Driver Impedance Control |
|---|---|
| 0 | Full strength |
| 1 | Reduced strength |

| A9 | A8 | A7 | OCD Calibration Program |
|---|---|---|---|
| 0 | 0 | 0 | OCD Calibration mode exit; maintain setting |
| 0 | 0 | 1 | Drive(1) |
| 0 | 1 | 0 | Drive(0) |
| 1 | 0 | 0 | Adjust mode[a] |
| 1 | 1 | 1 | OCD Calibration default [b] |

a : When Adjust mode is issued, AL from previously set value must be applied.
b : After setting to default, OCD mode needs to be exited by setting A9-A7 to 000.

| A5 | A4 | A3 | Additive Latency |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| A12 | Qoff (Optional)[a] |
|---|---|
| 0 | Output buffer enabled |
| 1 | Output buffer disabled |

a : Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s, RDQS, $\overline{\text{RDQS}}$. This feature is used in conjunction with dimm IDD measurements when IDDQ is not desired to be included.

| A10 | $\overline{\text{DQS}}$ |
|---|---|
| 0 | Enable |
| 1 | Disable |

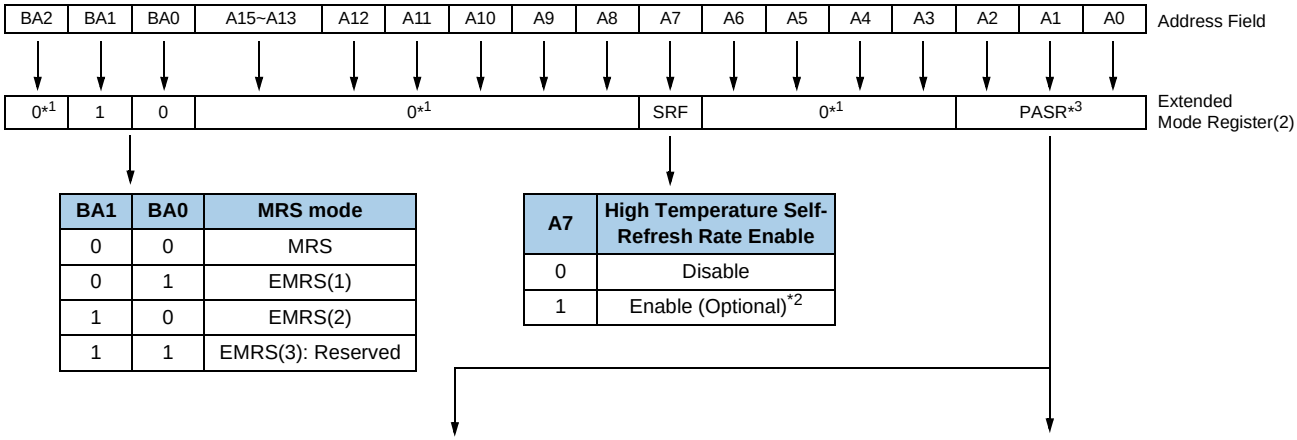
| A11 | RDQS Enable |
|---|---|
| 0 | Disable |
| 1 | Enable |

* If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

| A11 (RDQS Enable) | A10 ($\overline{\text{DQS}}$ Enable) | Strobe Function Matrix | | | |
|---|---|---|---|---|---|
| | | RDQS/DM | $\overline{\text{RDQS}}$ | DQS | $\overline{\text{DQS}}$ |
| 0 (Disable) | 0 (Enable) | DM | Hi-z | DQS | $\overline{\text{DQS}}$ |
| 0 (Disable) | 1 (Disable) | DM | Hi-z | DQS | Hi-z |
| 1 (Enable) | 0 (Enable) | RDQS | $\overline{\text{RDQS}}$ | DQS | $\overline{\text{DQS}}$ |
| 1 (Enable) | 1 (Disable) | RDQS | Hi-z | DQS | Hi-z |

*1 : BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

## EMRS(2) Programming




| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2) |
| 1 | 1 | EMRS(3): Reserved |

| A7 | High Temperature Self-Refresh Rate Enable |
|---|---|
| 0 | Disable |
| 1 | Enable (Optional)*2 |

| A2 | A1 | A0 | Partial Array Self Refresh for 8 Banks |
|---|---|---|---|
| 0 | 0 | 0 | Full Array |
| 0 | 0 | 1 | Half Array(BA[2:0]=000,001,010&011) |
| 0 | 1 | 0 | Quarter Array(BA[2:0]=000&001) |
| 0 | 1 | 1 | 1/8th Array(BA[2:0]=000) |
| 1 | 0 | 0 | 3/4 Array(BA[2:0]=010,011,100,101,110&111) |
| 1 | 0 | 1 | Half Array(BA[2:0]=100,101,110&111) |
| 1 | 1 | 0 | Quarter Array(BA[2:0]=110&111) |
| 1 | 1 | 1 | 1/8th Array(BA[2:0]=111) |

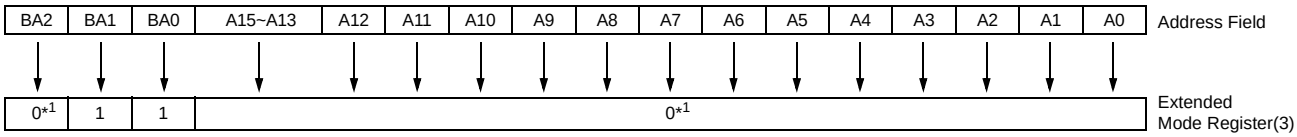
| A2 | A1 | A0 | Partial Array Self Refresh for 4 Banks |
|---|---|---|---|
| 0 | 0 | 0 | Full Array |
| 0 | 0 | 1 | Half Array(BA[1:0]=00&01) |
| 0 | 1 | 0 | Quarter Array(BA[1:0]=00) |
| 0 | 1 | 1 | Not defined |
| 1 | 0 | 0 | 3/4 Array(BA[1:0]=01,10&11) |
| 1 | 0 | 1 | Half Array(BA[1:0]=10&11) |
| 1 | 1 | 0 | Quarter Array(BA[1:0]=11) |
| 1 | 1 | 1 | Not defined |

*1 : The rest bits in EMRS(2) is reserved for future use and all bits in EMRS(2) except A0-A2, A7, BA0 and BA1 must be programmed to 0 when setting the extended mode register(2) during initialization.

*2 : Due to the migration natural, user needs to ensure the DRAM part supports higher than 85'C Tcase temperature self-refresh entry. JEDEC standard DDR2 SDRAM Module user can look at DDR2 SDRAM Module SPD field Byte 49 bit [0]. If the high temperature self-refresh mode is supported then controller can set the EMRS2[A7] bit to enable the self-refresh rate in case of higher than 85'C temperature self-refresh operation. For the loose part user, please refer to DRAM Manufacturer's part number and specification to check the high temperature self-refresh rate availability.

*3 : Optional in DDR2 SDRAM. If PASR(Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified location will be loast if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued.

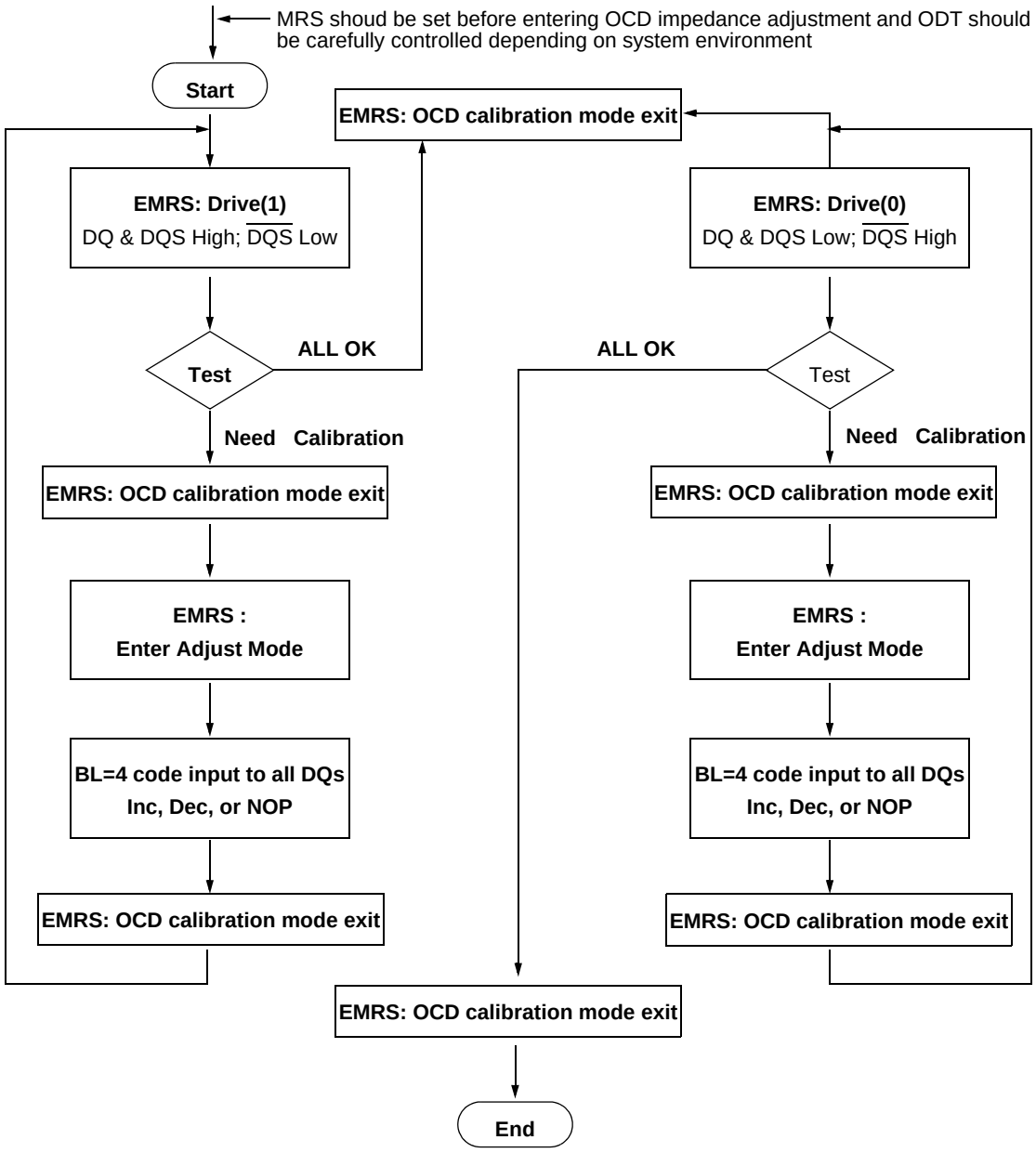
## EMRS(3) Programming: Reserved*1




*1 : All bits in EMRS(3) except BA0 and BA1 are reserved for future use and must be programmed to 0 when setting the mode register during initialization.

## Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



## Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in the table. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Off- Chip-Driver program

| A9 | A8 | A7 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | OCD calibration mode exit |
| 0 | 0 | 1 | Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ low |
| 0 | 1 | 0 | Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$ high |
| 1 | 0 | 0 | Adjust mode |
| 1 | 1 | 1 | OCD calibration default |

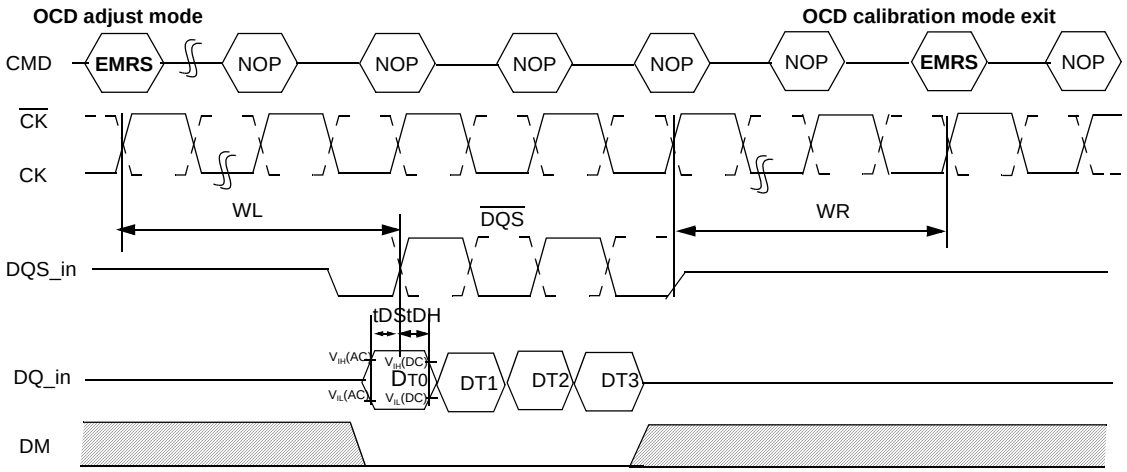
## OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in the folowing table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in the following table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Off- Chip-Driver Program

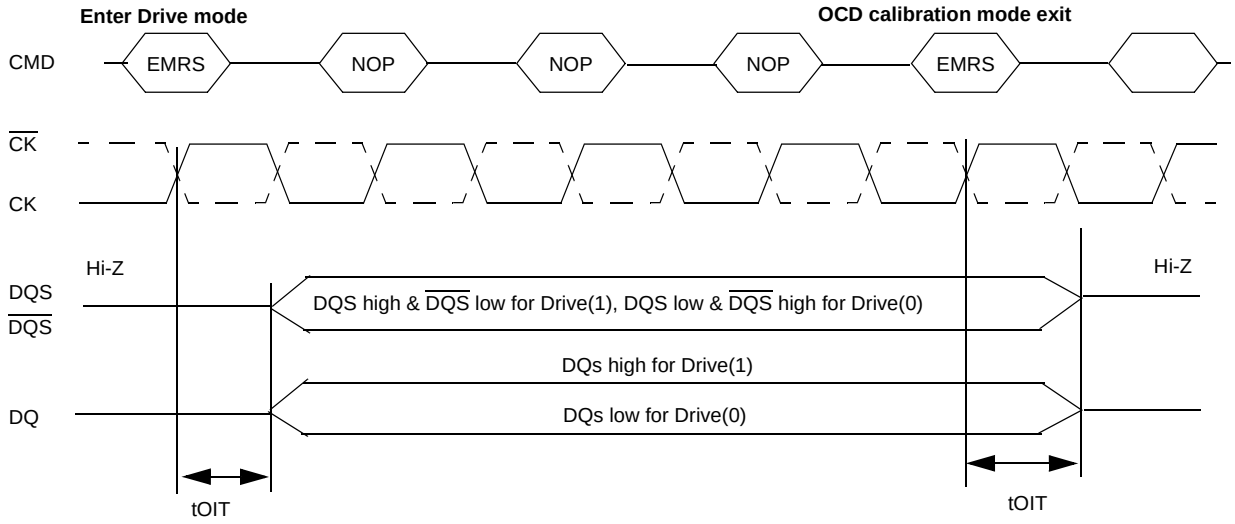
| 4bit burst code inputs to all DQs | | | | Operation | |
|---|---|---|---|---|---|
| $DT_0$ | $DT_1$ | $DT_2$ | $DT_3$ | Pull-up driver strength | Pull-down driver strength |
| 0 | 0 | 0 | 0 | NOP (No operation) | NOP (No operation) |
| 0 | 0 | 0 | 1 | Increase by 1 step | NOP |
| 0 | 0 | 1 | 0 | Decrease by 1 step | NOP |
| 0 | 1 | 0 | 0 | NOP | Increase by 1 step |
| 1 | 0 | 0 | 0 | NOP | Decrease by 1 step |
| 0 | 1 | 0 | 1 | Increase by 1 step | Increase by 1 step |
| 0 | 1 | 1 | 0 | Decrease by 1 step | Increase by 1 step |
| 1 | 0 | 0 | 1 | Increase by 1 step | Decrease by 1 step |
| 1 | 0 | 1 | 0 | Decrease by 1 step | Decrease by 1 step |
| Other Combinations | | | | Reserved | |

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as the following timing diagram. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by MRS addressing mode (ie. sequential or interleave).




## Drive Mode

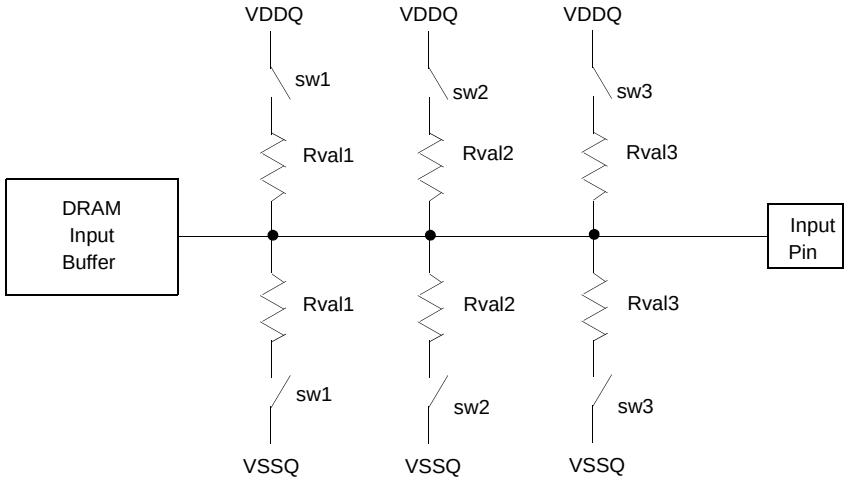
Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the following timing diagram.



## ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, and DM signal for x4/x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.
The ODT function is supported for ACTIVE and STANDBY modes, and turned off and not supported in SELF REFRESH mode.

## Functional Representation of ODT




Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2 and sw3 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

## ODT DC Electrical Characteristics

| Parameter/Condition | Symbol | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm | Rtt1(eff) | 60 | 75 | 90 | ohm | 1 |
| Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm | Rtt2(eff) | 120 | 150 | 180 | ohm | 1 |
| Rtt mismatch tolerance between any pull-up/pull-down pair | Rtt(mis) | -3.75 | | +3.75 | % | 1 |

Note 1 : Test condition for Rtt measurements

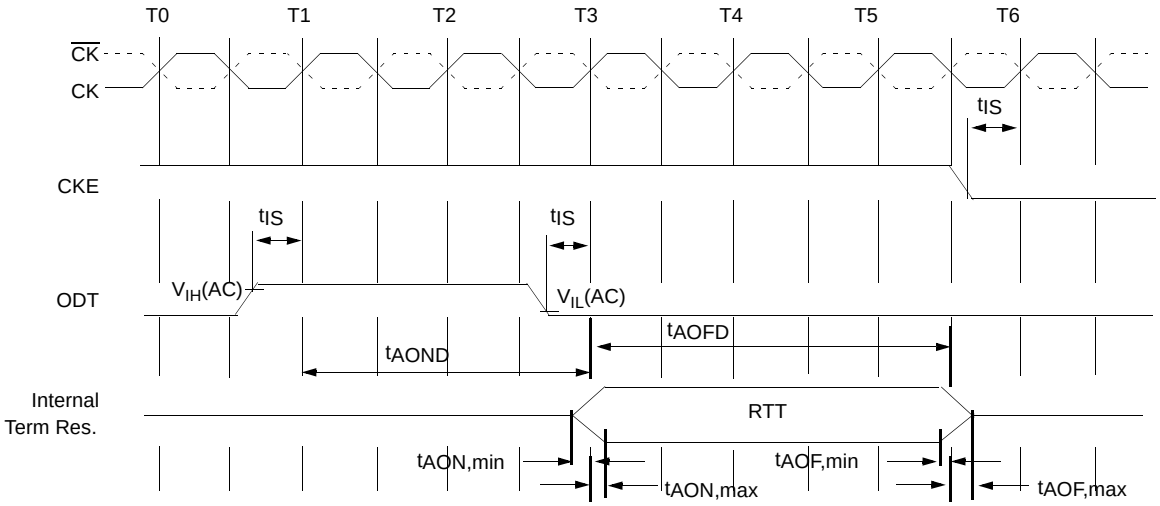
**Measurement Definition for Rtt(eff) :** Apply $V_{IH}$ (AC) and $V_{IL}$ (AC) to test pin separately, then measure current I($V_{IH}$ (AC)) and I( $V_{IL}$ (AC)) respectively. $V_{IH}$ (AC), $V_{IL}$ (AC), and VDDQ values defined in SSTL_18

$$Rtt(eff) = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

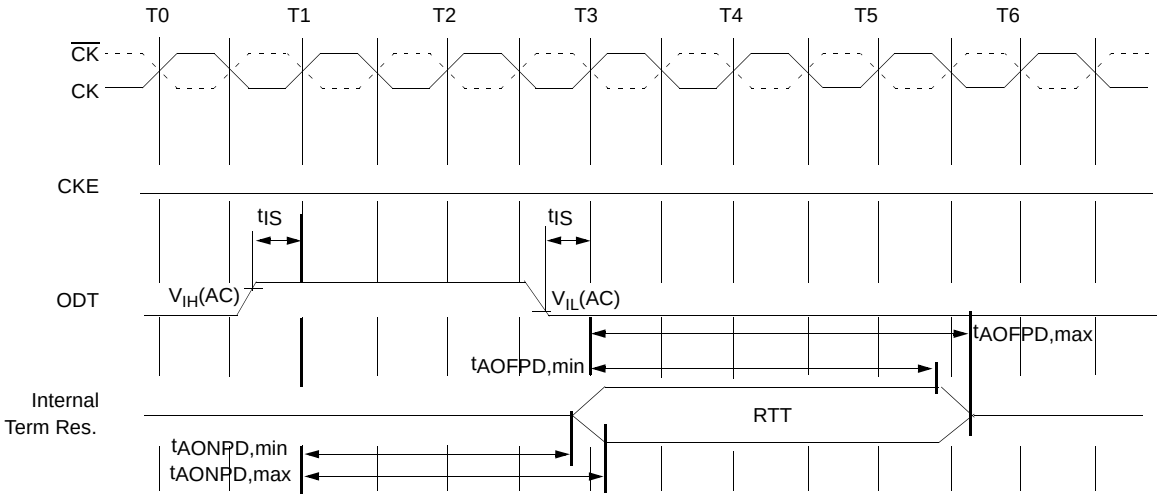
**Measurement Definition for VM :** Measure voltage ($V_M$) at test pin (midpoint) with no load.

$$\text{delta VM} = \left( \frac{2 \times Vm}{VDDQ} - 1 \right) \times 100\%$$

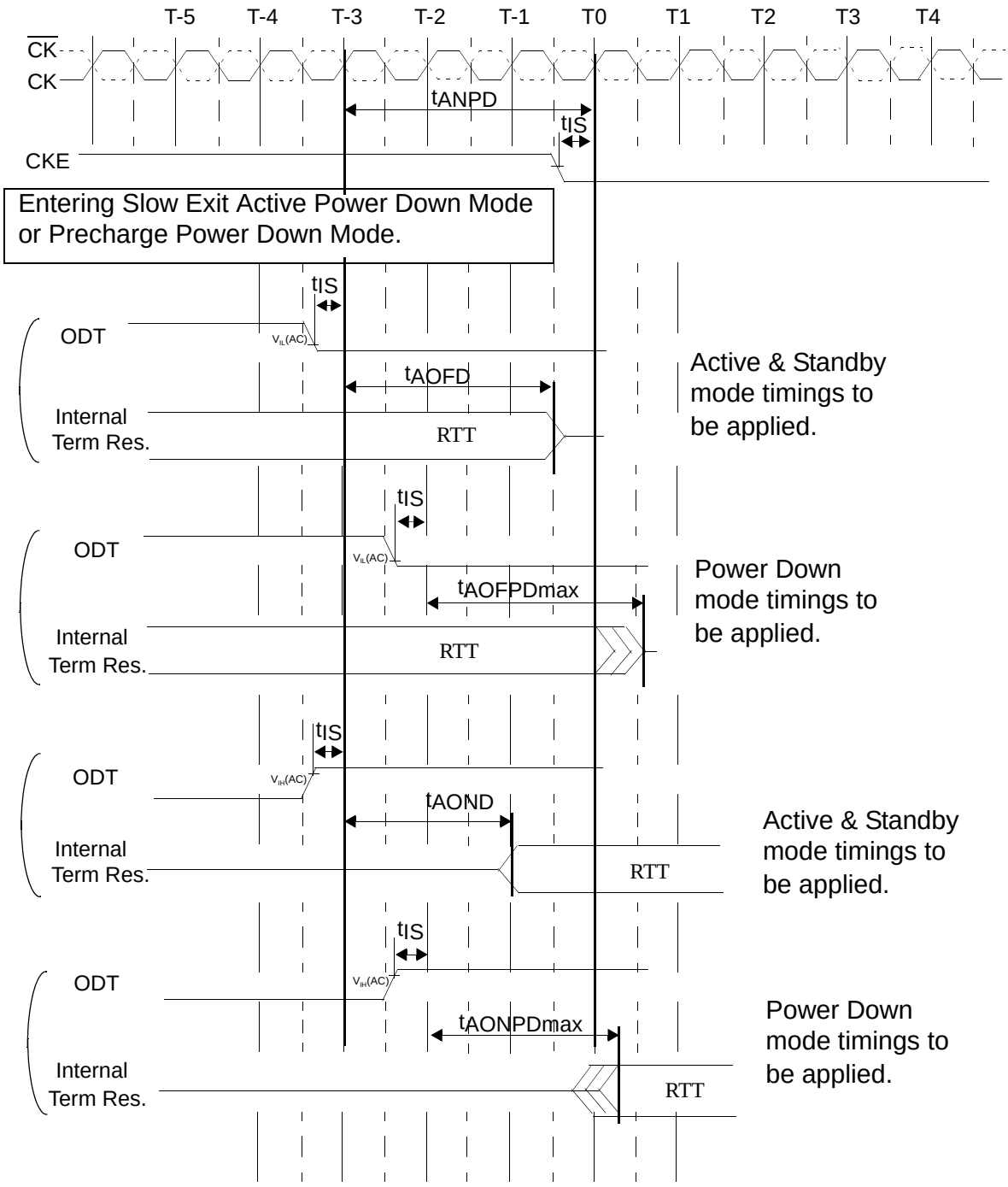
### ODT timing for active/standby mode



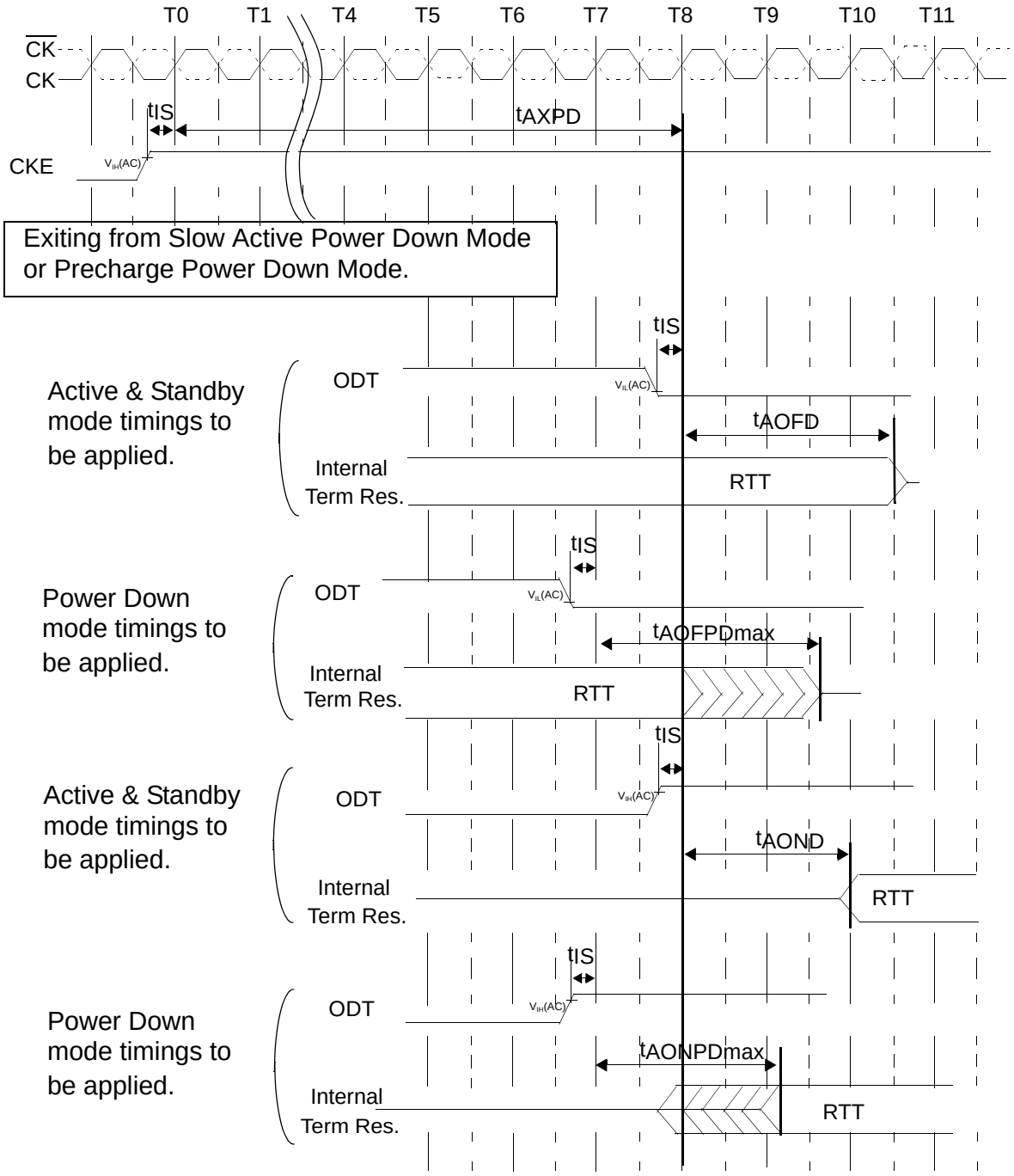

### ODT timing for powerdown mode



### ODT timing mode switch at entering power down mode



### ODT timing mode switch at exiting power down mode



### Bank Activate Command

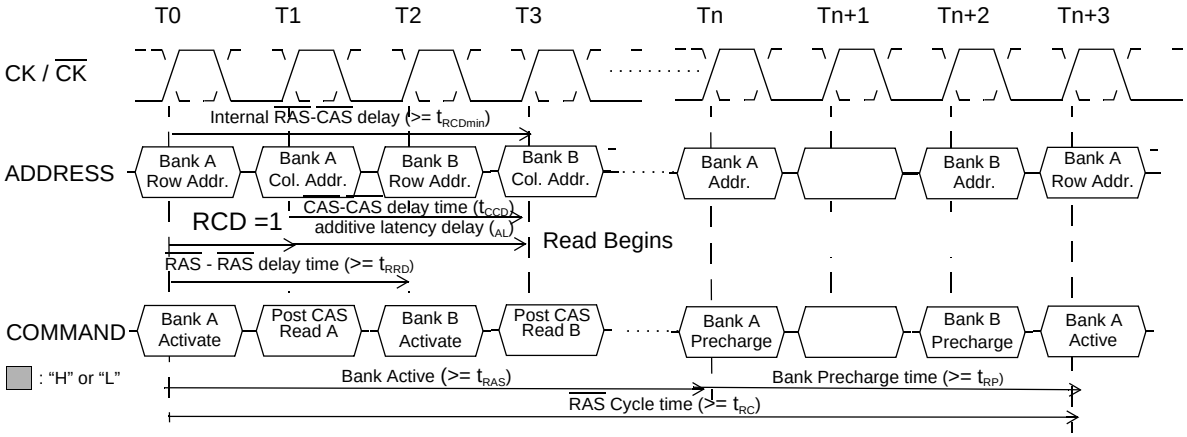
The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 and BA1, are used to select the desired bank. The row address A0 through A13 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device ($t_{RC}$). The minimum time interval between Bank Activate commands is $t_{RRD}$.

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

• 8 bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW(ns) by tCK(ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

• 8 bank device Precharge All Allowance : tRP for a Precharge All command for an 8 Bank device will equal to tRP + 1 * tCK, where tRP is the value for a single bank pre-charge.

**Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2**




### Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).
The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8 bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.
A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundry respectively. The minimum CAS to CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles. Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

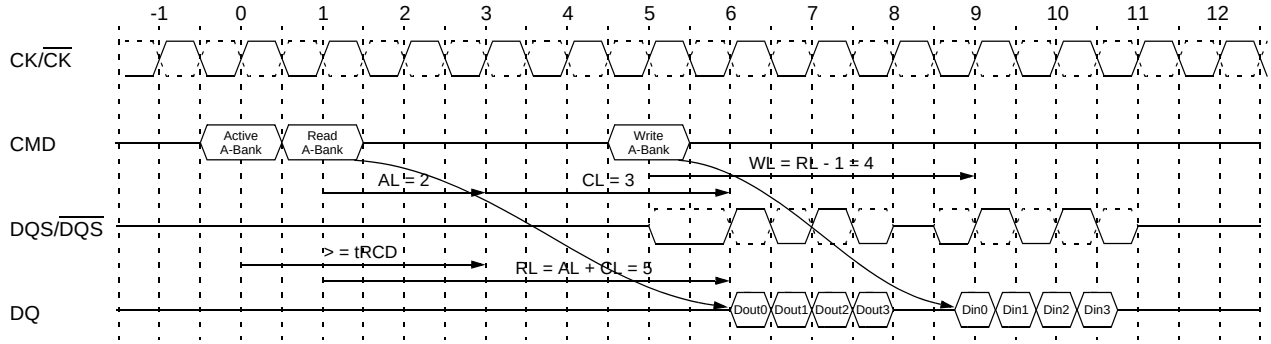
### Posted CAS

Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a CAS read or write command to be issued immediately after the RAS bank activate command (or any time during the RAS-CAS-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMR(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section)

## Examples of posted CAS operation

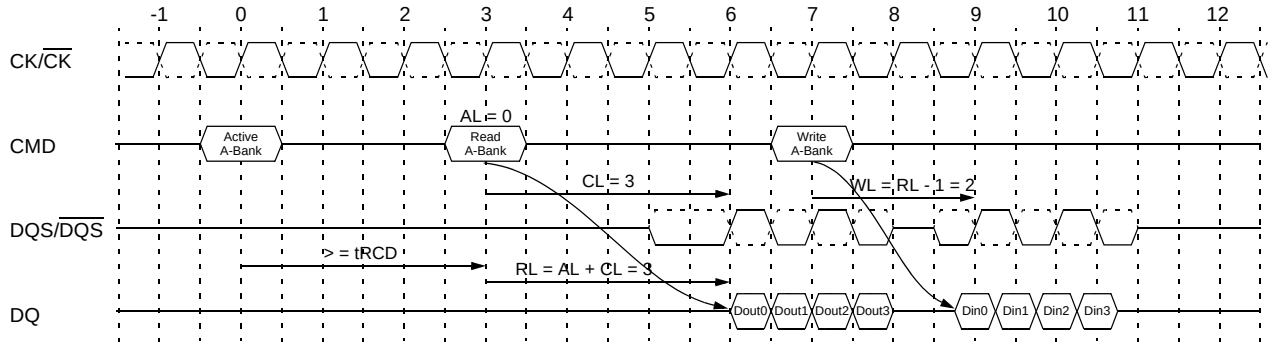
Example 1 Read followed by a write to the same bank

[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]




Example 2 Read followed by a write to the same bank

[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]



## Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.
Burst Length and Sequence

BL = 4

| Burst Length | Starting Address (A1 A0) | Sequential Addressing (decimal) | Interleave Addressing (decimal) |
|---|---|---|---|
| 4 | 0 0 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | 0 1 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | 1 0 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | 1 1 | 3, 0, 1, 2 | 3, 2, 1, 0 |

BL = 8

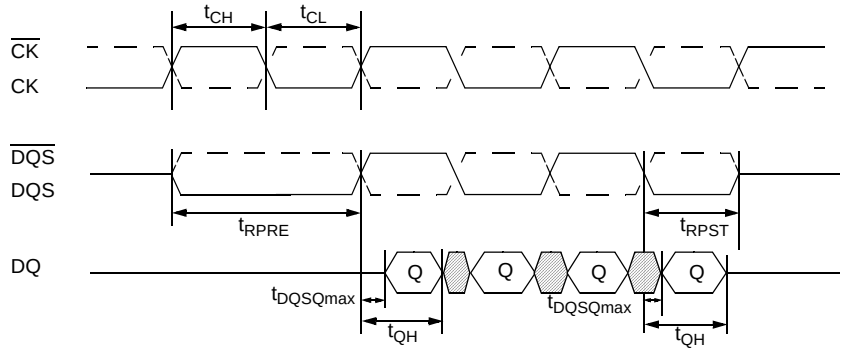
| Burst Length | Starting Address (A2 A1 A0) | Sequential Addressing (decimal) | Interleave Addressing (decimal) |
|---|---|---|---|
| 8 | 0 0 0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 0 0 1 | 1, 2, 3, 0, 5, 6, 7, 4 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 0 1 0 | 2, 3, 0, 1, 6, 7, 4, 5 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 0 1 1 | 3, 0, 1, 2, 7, 4, 5, 6 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 1 0 0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 1 0 1 | 5, 6, 7, 4, 1, 2, 3, 0 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 1 1 0 | 6, 7, 4, 5, 2, 3, 0, 1 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 1 1 1 | 7, 4, 5, 6, 3, 0, 1, 2 | 7, 6, 5, 4, 3, 2, 1, 0 |

Note : Page length is a function of I/O organization and column addressing.

## Burst Read Command

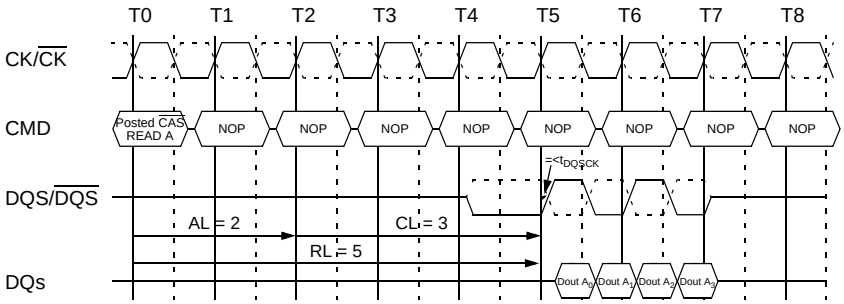
The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1)(EMRS(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differen-tial mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resis-tor to insure proper operation.

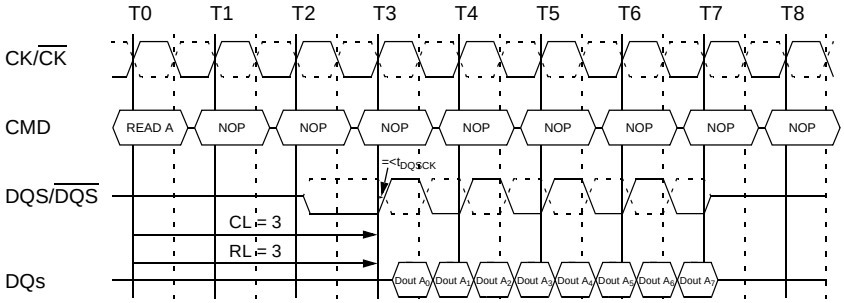



**Data output (read) timing**

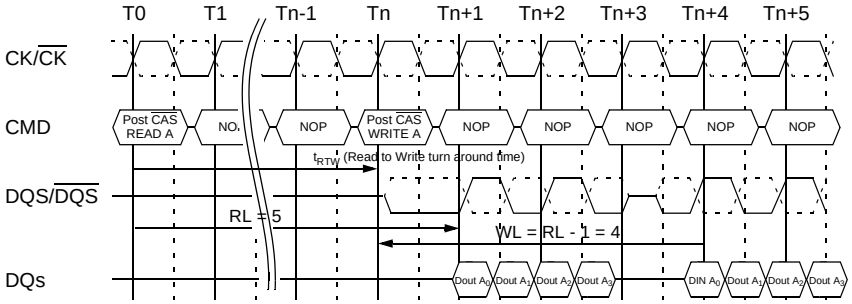
## Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)




## Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

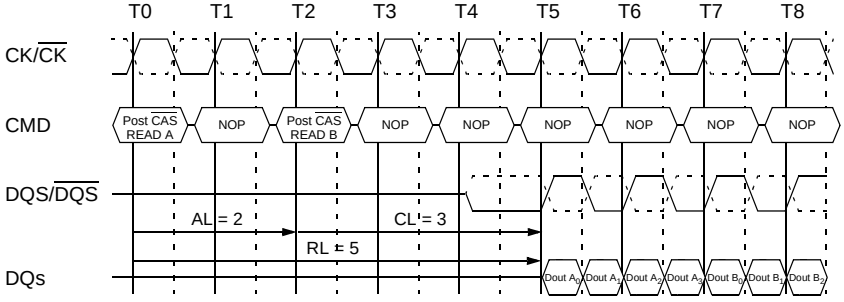



## Burst Read followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4




The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

## Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL=4

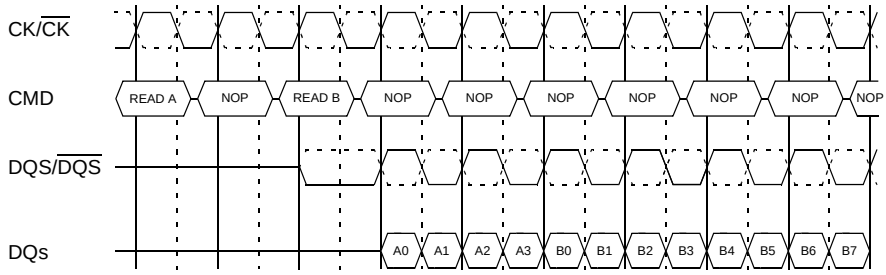



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

### Reads Interrupted by a Read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

### Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)

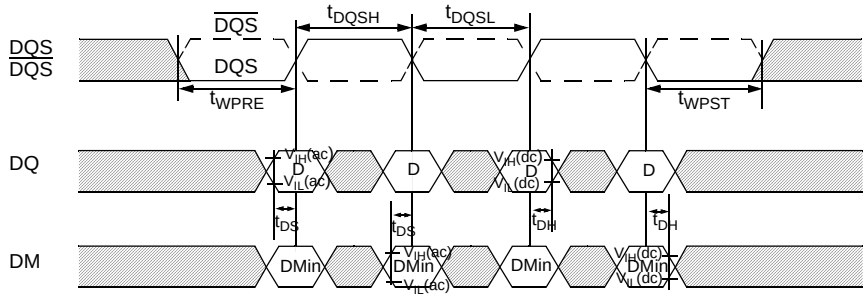



Notes:
1. Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
3. Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto Precharge enabled is not allowed to interrupt.
6. Read burst interruption is allowed by another Read with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

### Burst Write Operation

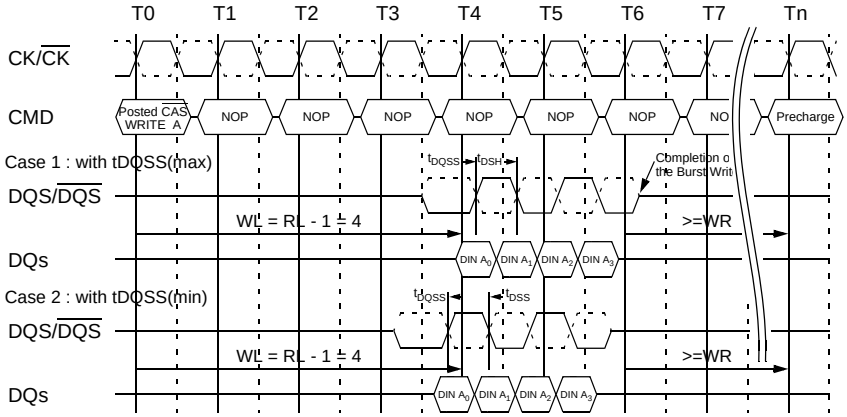
The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1);and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When t he burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at the specified AC/DC levels. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10K ohm resistor to insure proper operation.

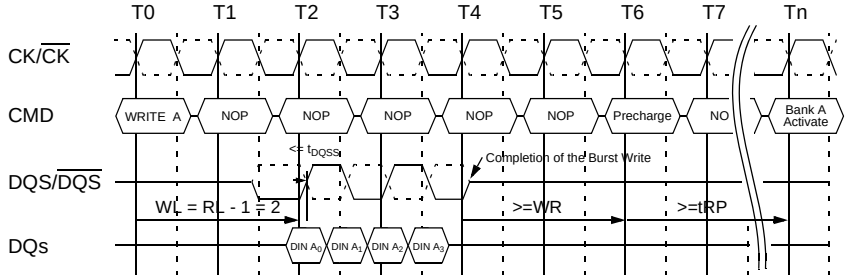



**Data input (write) timing**

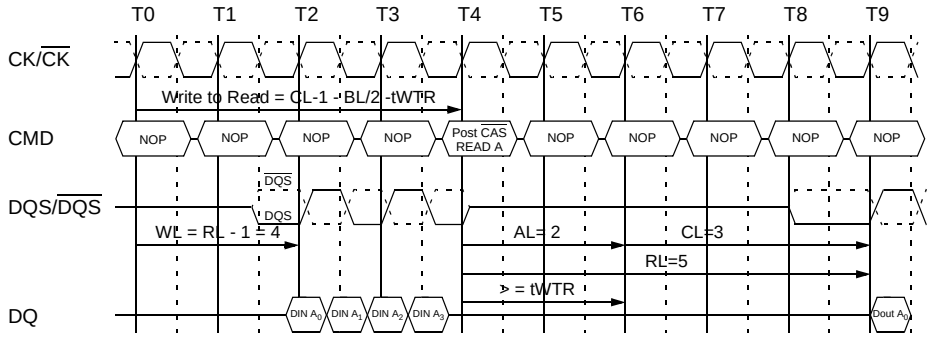
## Burst Write Operation: RL = 5, (AL=2, CL=3), WL = 4, WR = 3, BL = 4




## Burst Write Operation: RL = 3, (AL=0, CL=3), WL = 2, WR = 2, BL = 4

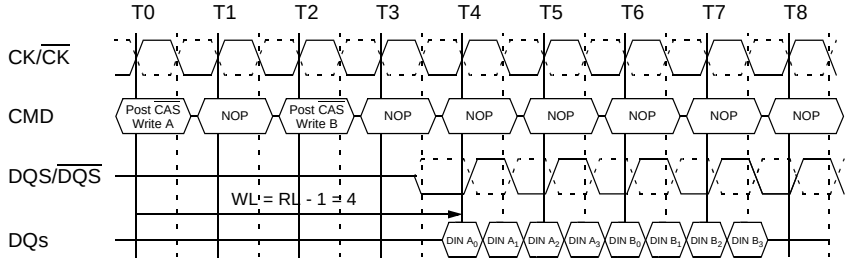



## Burst Write followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4




The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (WR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

## Seamless Burst Write Operation: RL = 5, WL = 4, BL=4

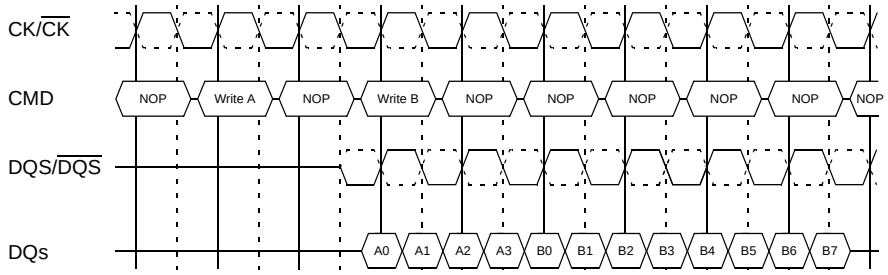



The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

### Writes intrrupted by a write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

### Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)

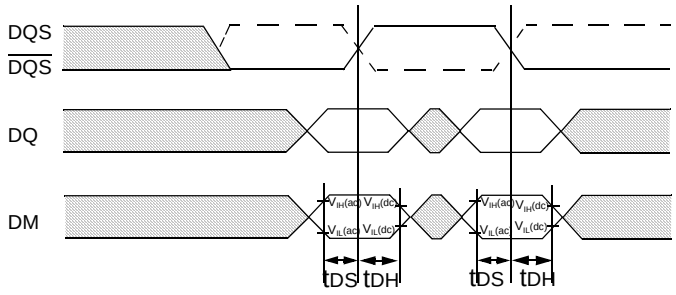



Notes:
1. Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.
3. Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto Precharge enabled is not allowed to interrupt.
6. Write burst interruption is allowed by another Write with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+WR where WR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

### Write data mask

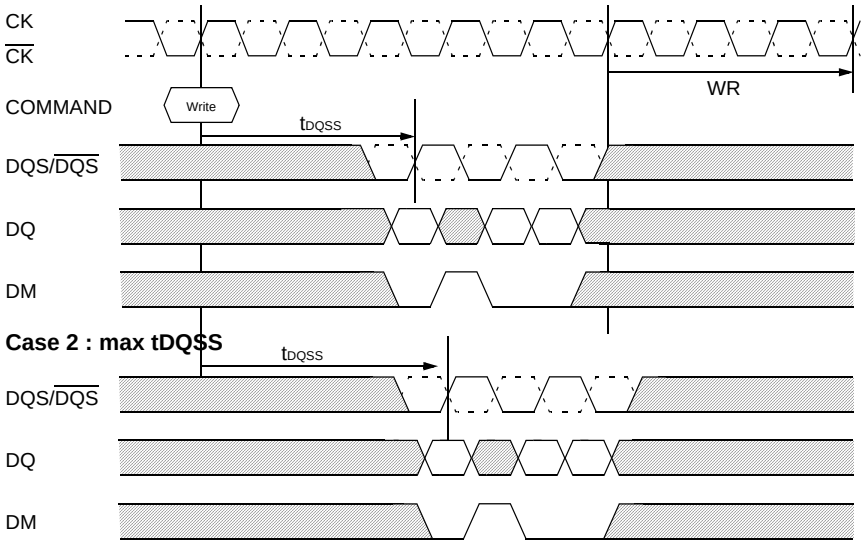
One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, Consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMRS(1) setting.

### Data Mask Timing




### Data Mask Function, WL=3, AL=0, BL = 4 shown

**Case 1 : min tDQSS**



### Precharge Operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 256Mb and 512Mb and four address bits A10, BA0 ~ BA2 for 1Gb and higher densities are used to define which bank to precharge when the command is issued. For 8 bank devices, refer to Bank Active section.

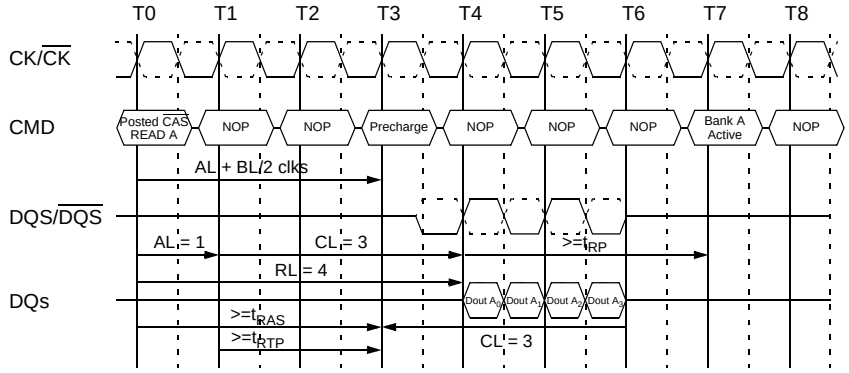
### Bank Selection for Precharge by Address Bits

| A10 | BA2 | BA1 | BA0 | Precharged Bank(s) | Remarks |
|---|---|---|---|---|---|
| LOW | LOW | LOW | LOW | Bank 0 only | |
| LOW | LOW | LOW | HIGH | Bank 1 only | |
| LOW | LOW | HIGH | LOW | Bank 2 only | |
| LOW | LOW | HIGH | HIGH | Bank 3 only | |
| LOW | HIGH | LOW | LOW | Bank 4 only | 1 Gb and higher |
| LOW | HIGH | LOW | HIGH | Bank 5 only | 1 Gb and higher |
| LOW | HIGH | HIGH | LOW | Bank 6 only | 1 Gb and higher |
| LOW | HIGH | HIGH | HIGH | Bank 7 only | 1 Gb and higher |
| HIGH | DON'T CARE | DON'T CARE | DON'T CARE | All Banks | |

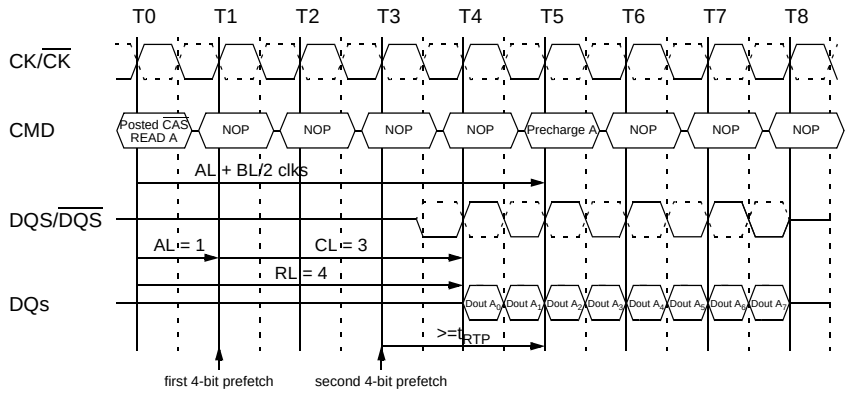
### Burst Read Operation Followed by Precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 + max(RTP, 2) - 2 clocks.
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time ($t_{RP}$). A precharge command cannot be issued until $t_{RAS}$ is satisfied.
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

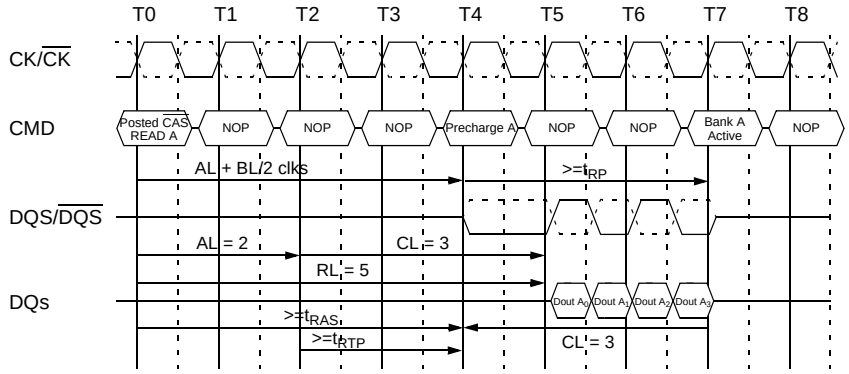
### Example 1 : Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 4, $t_{RTP}$ <= 2 clocks



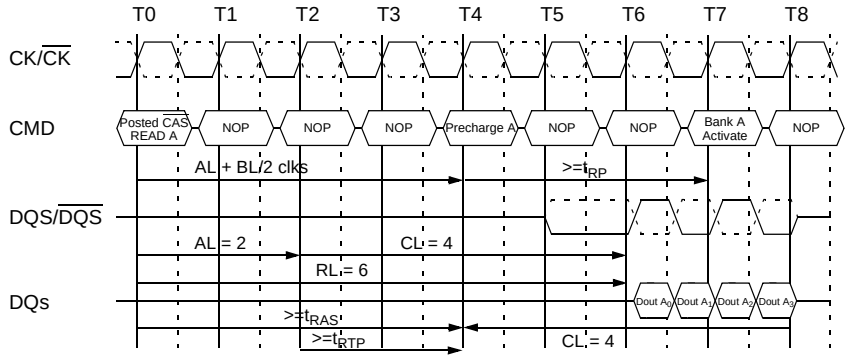

### Example 2 : Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, $t_{RTP}$ <= 2 clocks



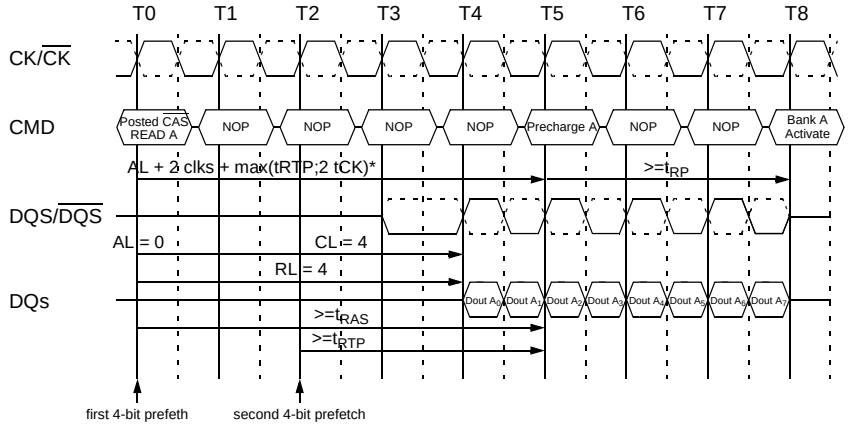
**Example 3: Burst Read Operation Followed by Precharge:**
**RL = 5, AL = 2, CL = 3, BL = 4, $t_{RTP}$ <= 2 clocks**




**Example 4: Burst Read Operation Followed by Precharge:**
**RL = 6, AL = 2, CL = 4, BL = 4, $t_{RTP}$ <= 2 clocks**




**Example 5: Burst Read Operation Followed by Precharge:**
**RL = 4, AL = 0, CL = 4, BL = 8, $t_{RTP}$ > 2 clocks**

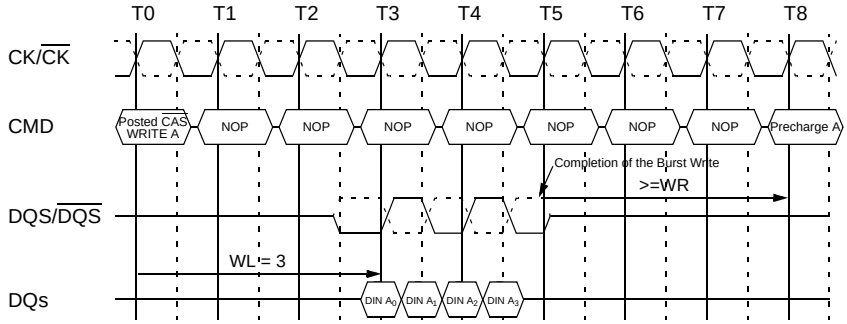



* : rounded to next integer.

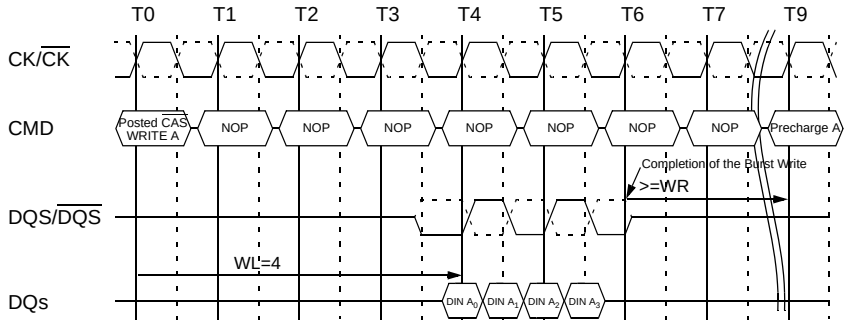
### Burst Write followed by Precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + WR For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (WR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the WR delay.

### Example 1: Burst Write followed by Precharge: WL = (RL-1) =3




### Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4



### Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst.
Auto-precharge also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.
This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read or write command.

### Burst Read with Auto Precharge

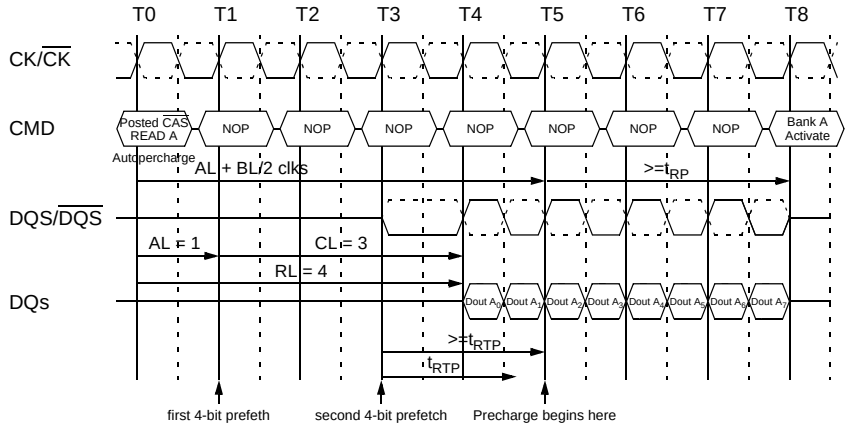
If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP are satisfied.

If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied.

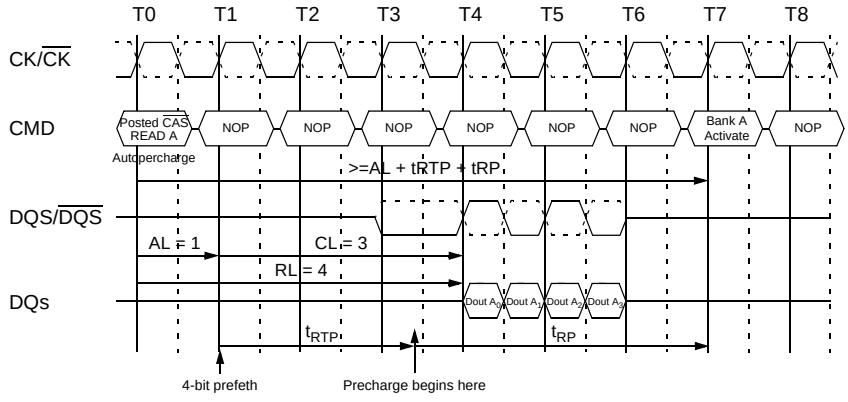
If tRTP(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRTP(min) is satisfied.
In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read_AP to the next Activate command becomes AL + (tRTP + tRP)* (see example 2) for BL = 8 the time from Read_AP to the next Activate is AL + 2 + (tRTP + tRP)*, where "*" means: "rouded up to the next integer". In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.
(1) The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

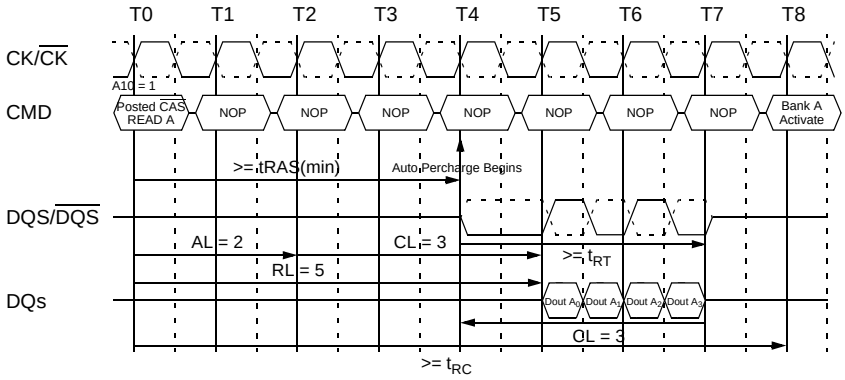
**Example 1: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 8, $t_{RTP}$ <= 2 clocks**



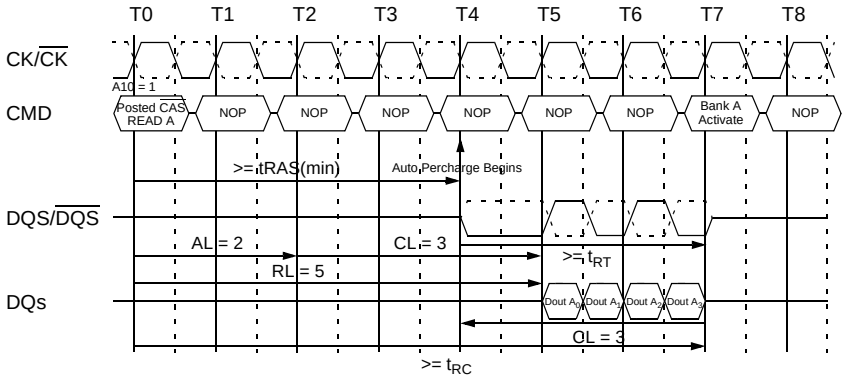

**Example 2: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 4, $t_{RTP}$ > 2 clocks**



**Example 3: Burst Read with Auto Precharge Followed by an activation to the Same Bank(tRC Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, $t_{RTP}$ <= 2 clocks)**



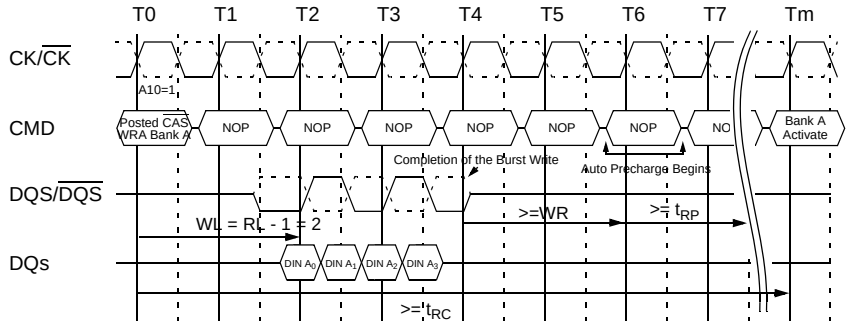

**Example 4: Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRP Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, $t_{RTP}$ <= 2 clocks)**



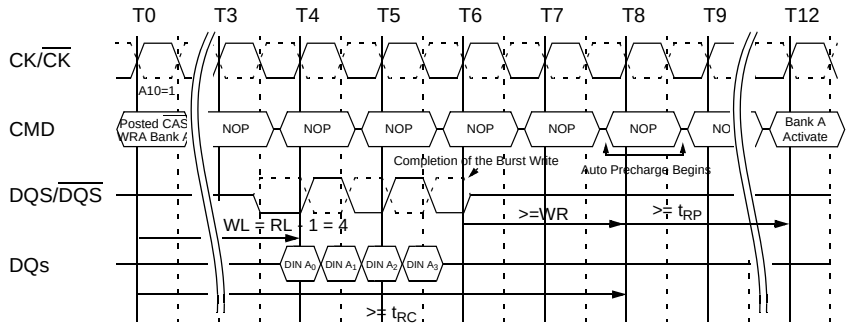
### Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.
(1) The data-in to bank activate delay time (WR + tRP) has been satisfied.
(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

## Burst Write with Auto-Precharge (tRC Limit): WL = 2, WR =2, tRP=3, BL=4




## Burst Write with Auto-Precharge (WR + tRP): WL = 4, WR =2, tRP=3, BL=4



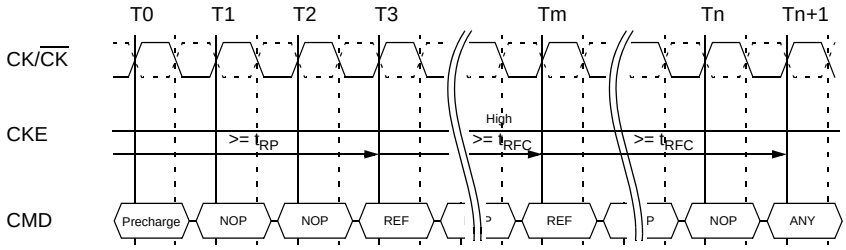
### Precharge & Auto Precharge Clarification

| From Command | To Command | Minimum Delay beween "From Command" to "To Command" | Unit | Notes |
|---|---|---|---|---|
| Read | Precharge ( to same Bank as Read ) | AL + BL/2 + max(RTP,2) - 2 | clks | 1, 2 |
| | Precharge All | AL + BL/2 + max(RTP,2) - 2 | clks | 1, 2 |
| Read w/AP | Precharge ( to same Bank as Read w/AP) | AL + BL/2 + max(RTP,2) - 2 | clks | 1, 2 |
| | Precharge All | AL + BL/2 + max(RTP,2) - 2 | clks | 1, 2 |
| Write | Precharge ( to same Bank as Write ) | WL + BL/2 + WR | clks | 2 |
| | Precharge All | WL + BL/2 + WR | clks | 2 |
| Write w/AP | Precharge ( to same Bank as Write w/AP) | WL + BL/2 + WR | clks | 2 |
| | Precharge All | WL + BL/2 + WR | clks | 2 |
| Precharge | Precharge ( to same Bank as Precharge) | 1 | clks | 2 |
| | Precharge All | 1 | clks | 2 |
| Precharge All | Precharge | 1 | clks | 2 |
| | Precharge All | 1 | clks | 2 |

Note :
1. RTP[cycles] = RU{tRTP(ns)/tCK(ns)}, where RU stands for round up.
2. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP or tRP all depending on the latest precharge command issued to that bank.

### Refresh Command

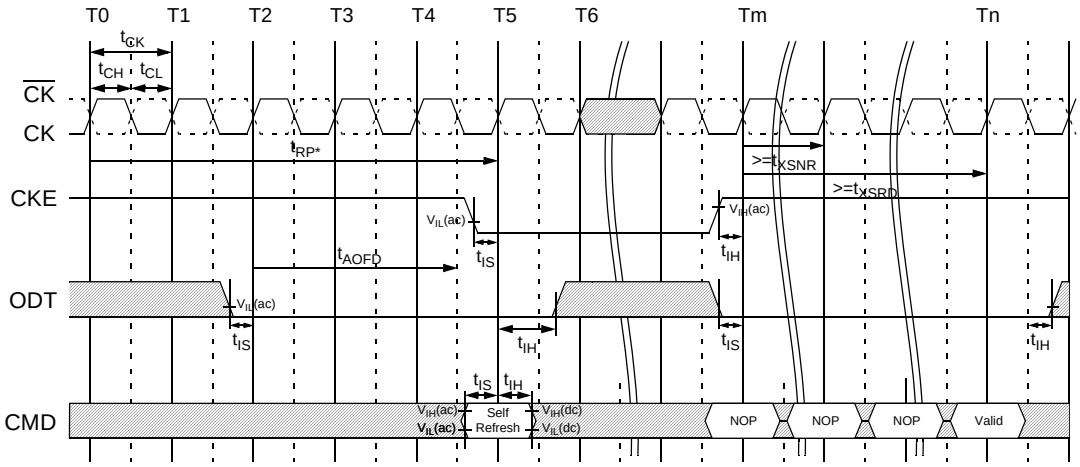
When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.
When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * tREFI.



### Self Refresh Operation

The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are "don't care". For proper Self Refresh operation all power supply pins (VDD, VDDQ, VDDL and Vref) must be at valid levels. The DRAM initiates a minimum of one refresh command internally within tCKE period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSNR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain high for the entire Self Refresh exit period tXSRD for proper operation except for Self Refresh re-entry. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least tXSNR period and issuing one refresh command(refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval tXSNR. ODT should be turned off during tXSRD. The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.



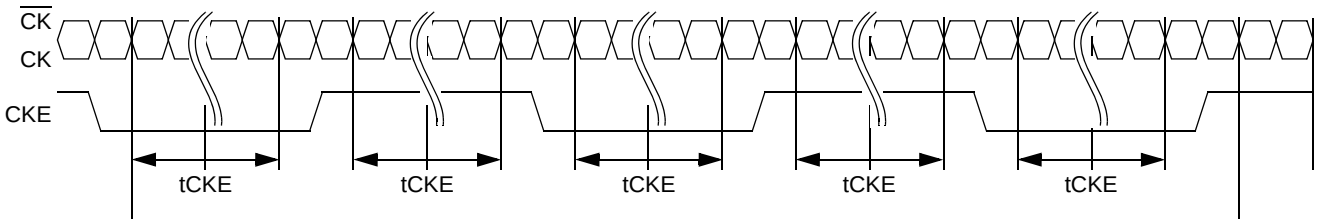

- Device must be in the "All banks idle" state prior to entering Self Refresh mode.
- ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.
- tXSRD is applied for a Read or a Read with autoprecharge command
- tXSNR is applied for any command except a Read or a Read with autoprecharge command.

### Power-Down

Power-down is synchronously entered when CKE is registered low (along with Nop or Deselect command). CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or autoprecharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

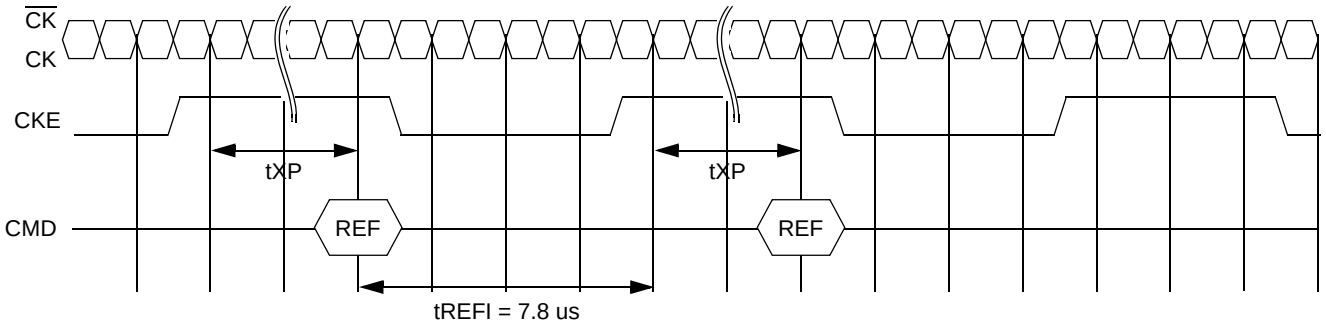
The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation. DRAM design guarantees all AC and DC timing & voltage specifications as well proper DLL operation with any CKE intensive operations as long as DRAM controller compliers with DRAM specifications. Following figures show two examples of CKE intensive applications.

<Example of CKE instensive environment 1>




DRAM guarantees all AC and DC timing & voltage specifications and proper DLL operation with intensive CKE operation

<Example of CKE intensive enviroment 2>

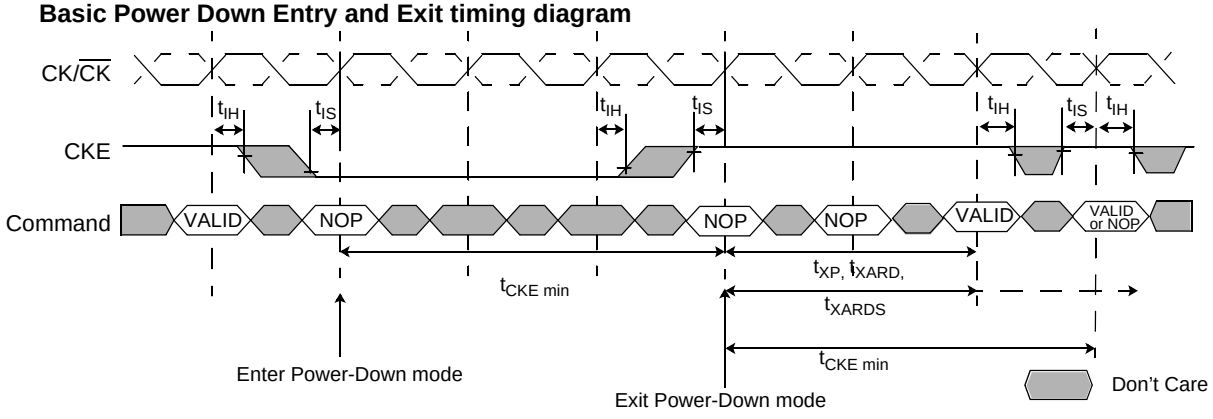



The pattern shown above can repeat over a long period of time. With this pattern, DRAM guarantees all DRAM guarantees all AC and DC timing & voltage specifications and DLL operation with temperature and voltage drift.

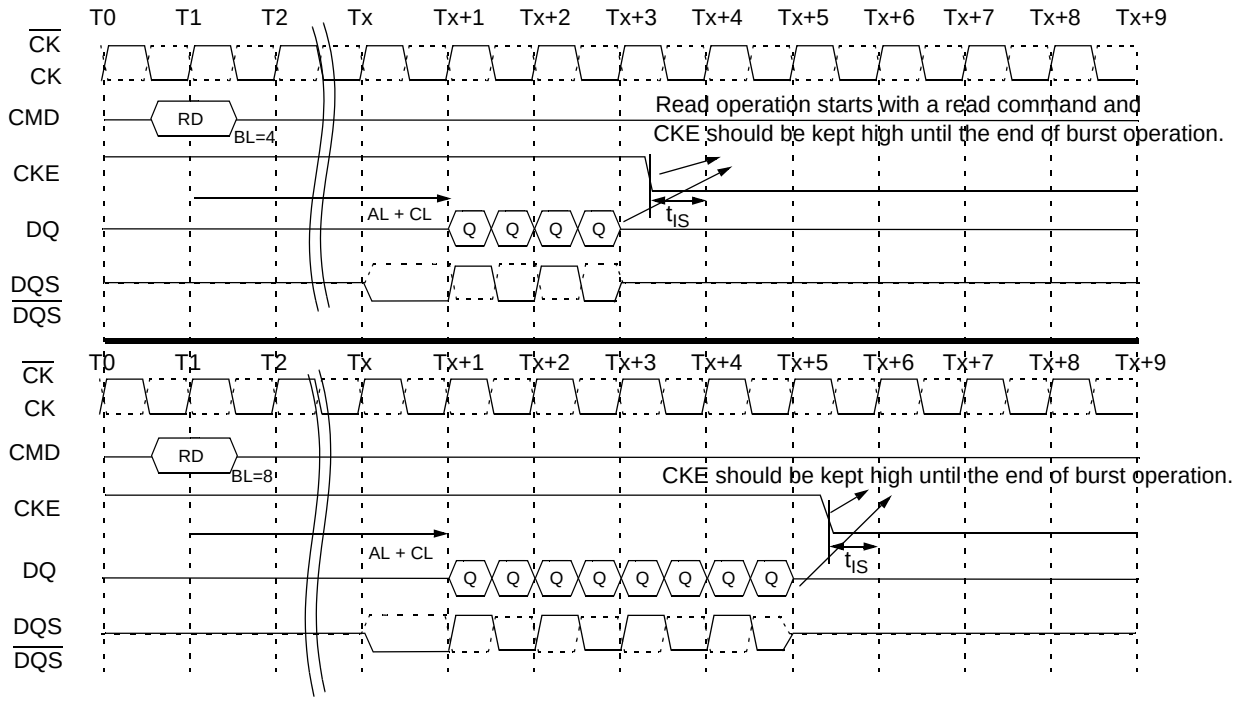
If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes high. Power-down exit latency is defined at AC spec table of this data sheet.

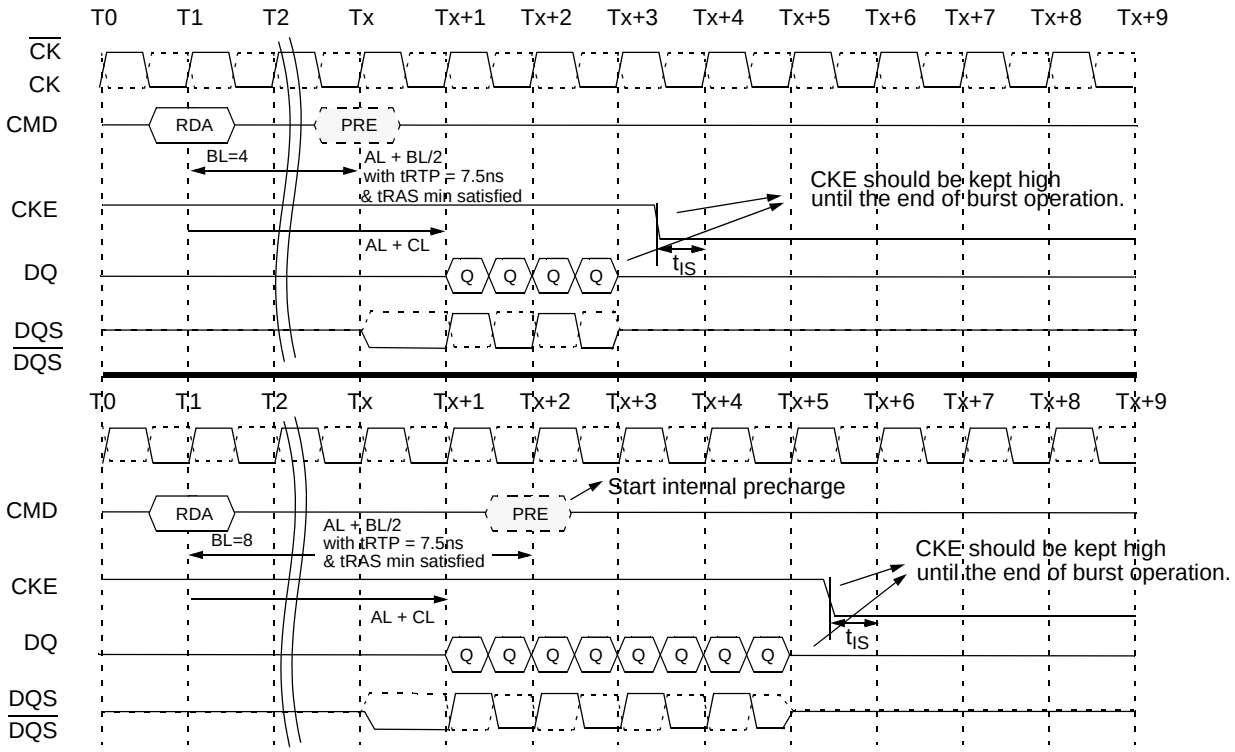
**Basic Power Down Entry and Exit timing diagram**



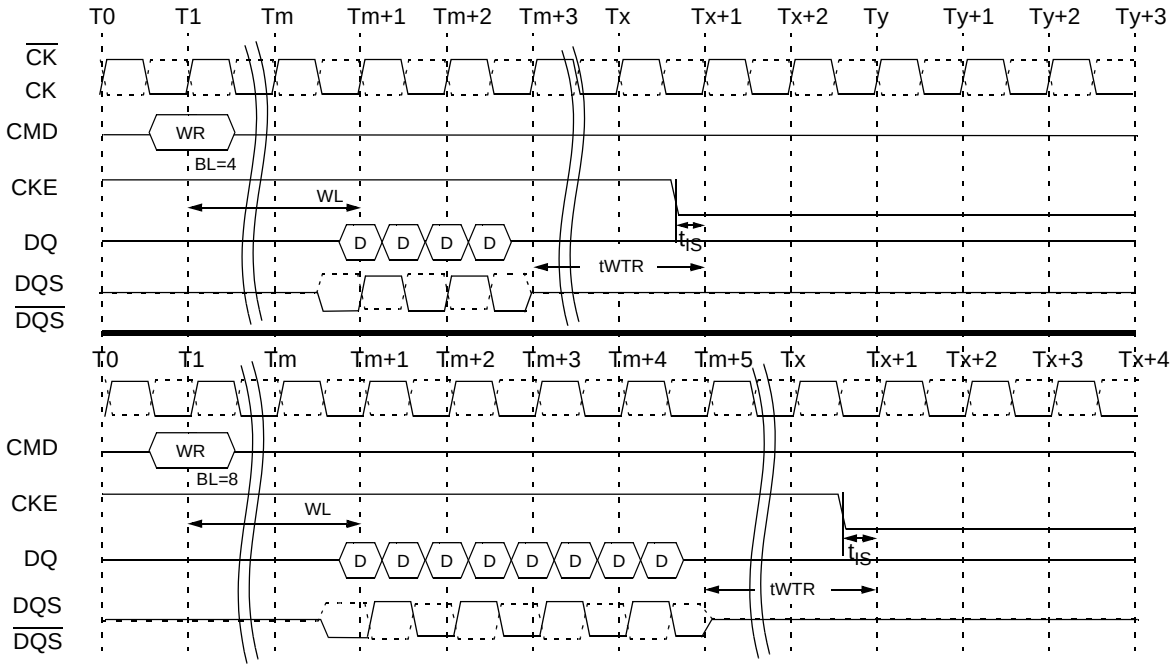
### Read to power down entry



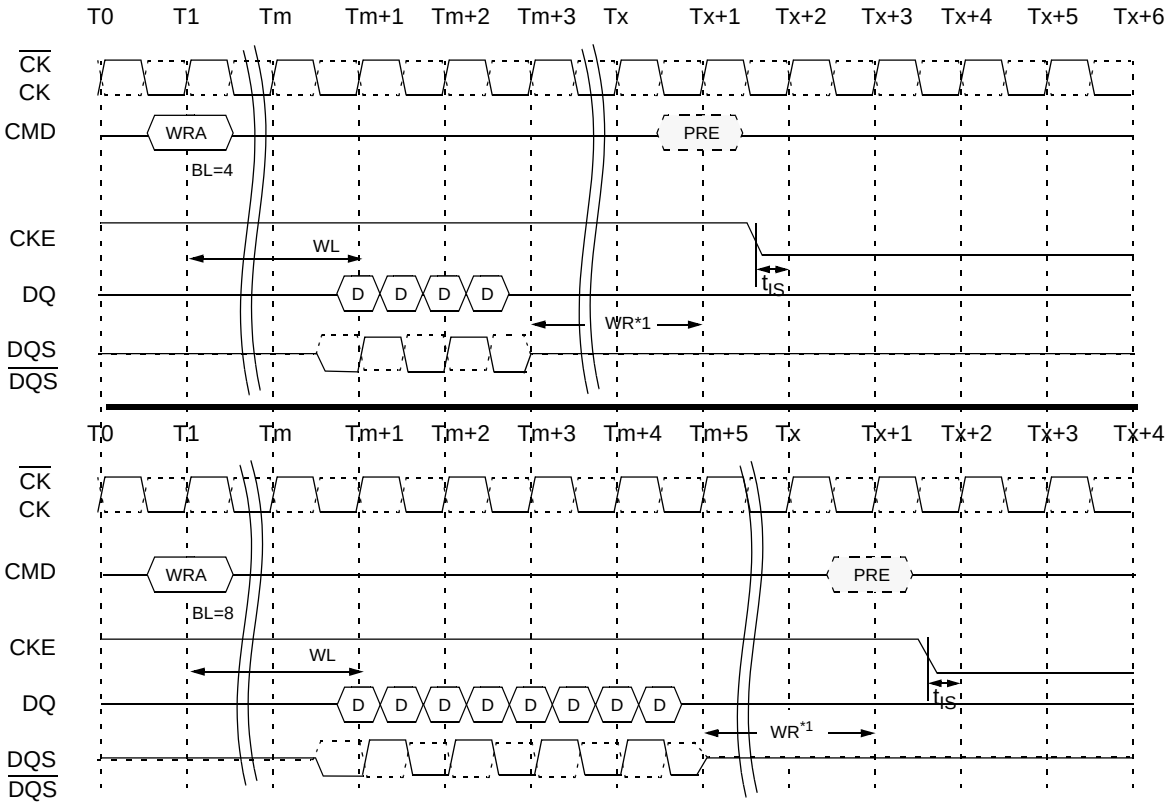

### Read with Autoprecharge to power down entry



### Write to power down entry

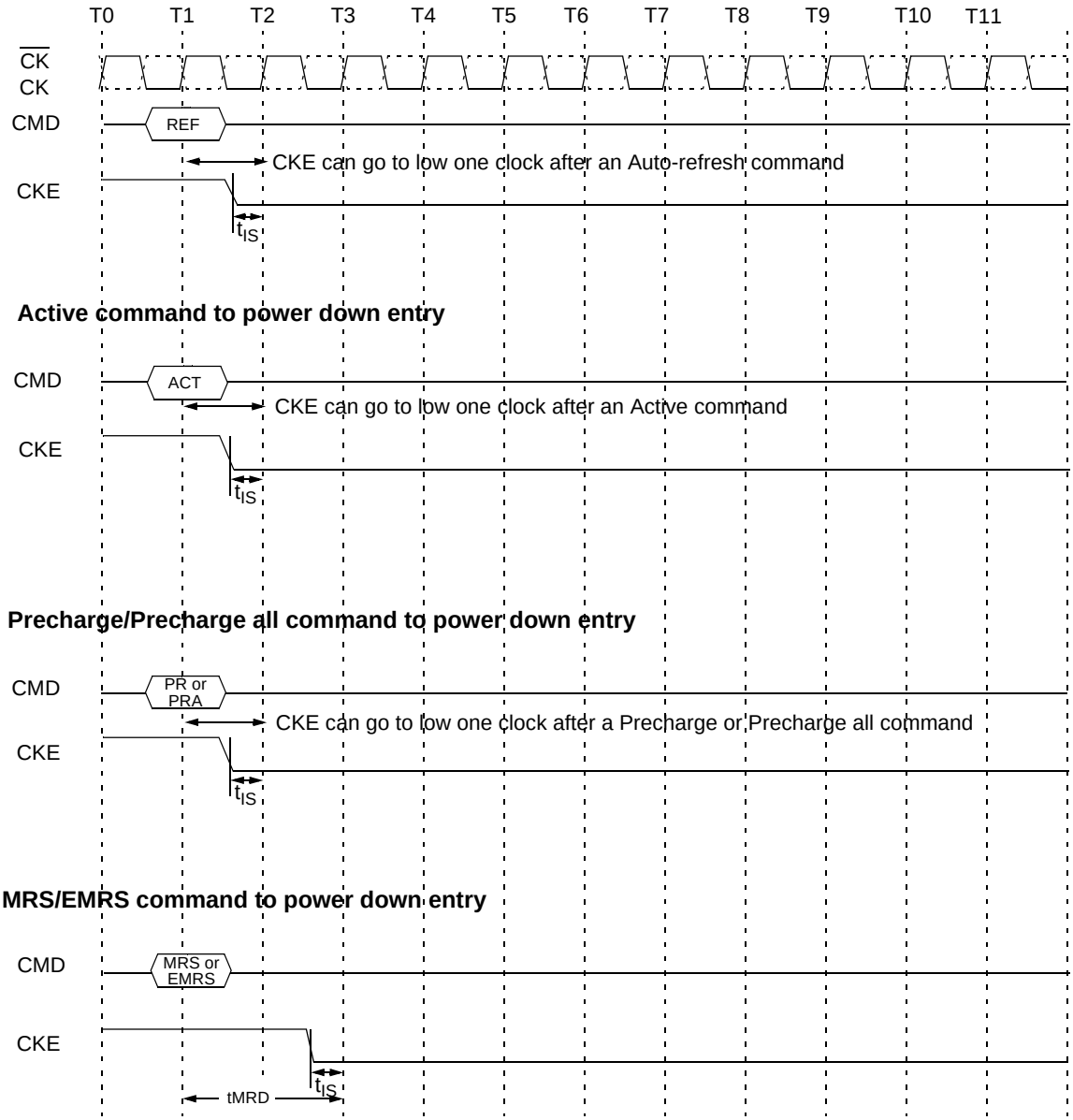



### Write with Autoprecharge to power down entry




* 1: WR is programmed through MRS

**Refresh command to power down entry**




**Active command to power down entry**



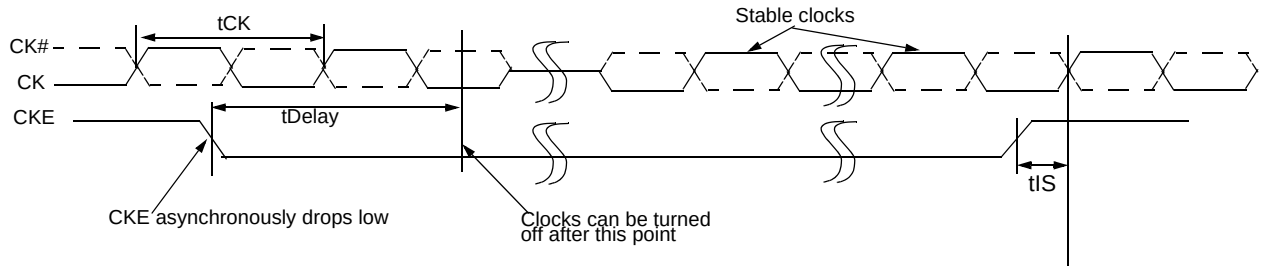

**Precharge/Precharge all command to power down entry**




**MRS/EMRS command to power down entry**

### Asynchronous CKE Low Event

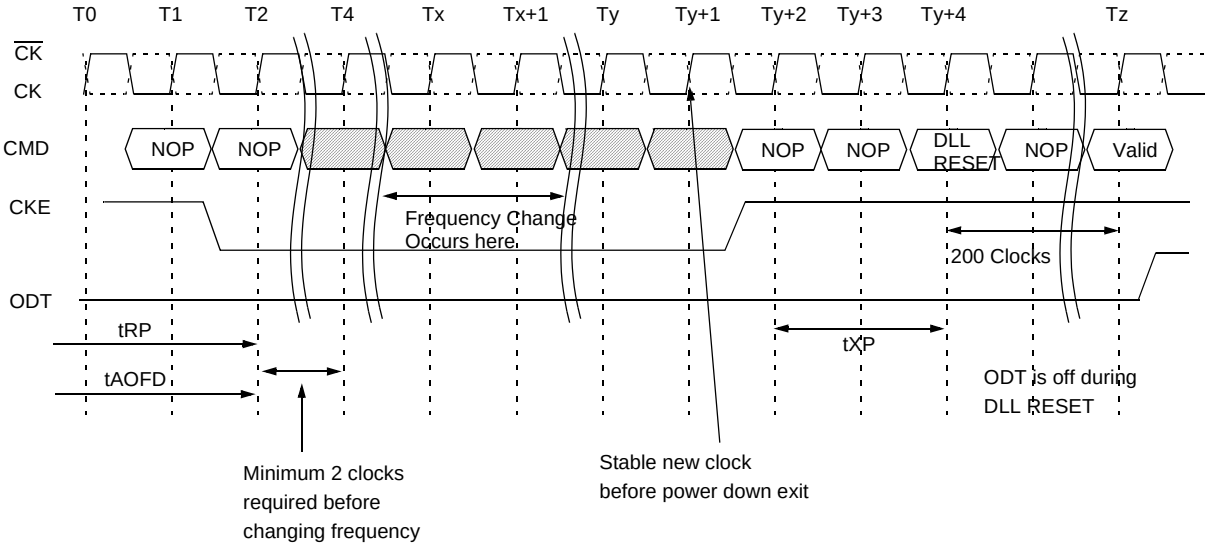
DRAM requires CKE to be maintained “HIGH” for all valid operations as defined in this data sheet. If CKE asynchronously drops “LOW” during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “HIGH” again. DRAM must be fully re-initialized (steps 4 thru 13) as described in initialization sequence. DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for tDelay specification.




### Input Clock Frequency Change during Precharge Power Down

DDR2 SDRAM input clock frequency can be changed under following condition:
DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc.. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

### Clock Frequency Change in Precharge Power Down Mode




### No Operation Command

The No Operation Command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation Command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

### Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don’t cares.

## Command Truth Table.

| Function | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0 BA1 BA2 | A15-A11 | A10 | A9 - A0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| (Extended) Mode Register Set | H | H | L | L | L | L | BA | OP Code | | | 1,2 |
| Refresh (REF) | H | H | L | L | L | H | X | X | X | X | 1 |
| Self Refresh Entry | H | L | L | L | L | H | X | X | X | X | 1 |
| Self Refresh Exit | L | H | H | X | X | X | X | X | X | X | 1,7 |
| | | | L | H | H | H | | | | | |
| Single Bank Precharge | H | H | L | L | H | L | BA | X | L | X | 1,2 |
| Precharge all Banks | H | H | L | L | H | L | X | X | H | X | 1 |
| Bank Activate | H | H | L | L | H | H | BA | Row Address | | | 1,2 |
| Write | H | H | L | H | L | L | BA | Column | L | Column | 1,2,3, |
| Write with Auto Precharge | H | H | L | H | L | L | BA | Column | H | Column | 1,2,3, |
| Read | H | H | L | H | L | H | BA | Column | L | Column | 1,2,3 |
| Read with Auto-Precharge | H | H | L | H | L | H | BA | Column | H | Column | 1,2,3 |
| No Operation | H | X | L | H | H | H | X | X | X | X | 1 |
| Device Deselect | H | X | H | X | X | X | X | X | X | X | 1 |
| Power Down Entry | H | L | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |
| Power Down Exit | L | H | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |

Note :
1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ , $\overline{WE}$ and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write"
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. “X” means “H or L (but a defined logic level)”.
7. Self refresh exit is asynchronous.
8. $V_{REF}$ must be maintained during Self Refresh operation.

### Clock Enable (CKE) Truth Table for Synchronous Transitions

| Current State [2] | CKE | | Command (N) [3] | Action (N) [3] | Notes |
|---|---|---|---|---|---|
| | Previous Cycle [1] (N-1) | Current Cycle [1] (N) | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$ | | |
| Power Down | L | L | X | Maintain Power-Down | 11, 13, 15 |
| | L | H | DESELECT or NOP | Power Down Exit | 4, 8, 11,13 |
| Self Refresh | L | L | X | Maintain Self Refresh | 11, 15 |
| | L | H | DESELECT or NOP | Self Refresh Exit | 4, 5,9 |
| Bank(s) Active | H | L | DESELECT or NOP | Active Power Down Entry | 4,8,10,11,13 |
| All Banks Idle | H | L | DESELECT or NOP | Precharge Power Down Entry | 4, 8, 10,11,13 |
| | H | L | REFRESH | Self Refresh Entry | 6, 9, 11,13 |
| | H | H | Refer to the Command Truth Table | | 7 |

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the $t_{XSNR}$ period. Read commands may be issued only after $t_{XSRD}$ (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section "Power Down" and "Self Refresh Command" for a detailed list of restrictions.
11. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2*tCK + tIH.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined.
14. CKE must be maintained high while the SDRAM is in OCD calibration mode .
15. “X” means “don’t care (including floating around $V_{REF}$)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMRS(1) ).
16. $V_{REF}$ must be maintained during Self Refresh operation.

### DM Truth Table

| Name (Functional) | DM | DQs | Note |
|---|---|---|---|
| Write enable | L | Valid | 1 |
| Write inhibit | H | X | 1 |

Note 1 : Used to mask write data, provided coincident with the corresponding data.

## Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | - 1.0 V ~ 2.3 V | V | 1 |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | - 0.5 V ~ 2.3 V | V | 1 |
| $V_{DDL}$ | Voltage on $V_{DDL}$ pin relative to $V_{SS}$ | - 0.5 V ~ 2.3 V | V | 1 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | - 0.5 V ~ 2.3 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1, 2 |

Note :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

## AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Supply Voltage | 1.7 | 1.8 | 1.9 | V | 1 |
| $V_{DDL}$ | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 5 |
| $V_{DDQ}$ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 1, 5 |
| $V_{REF}$ | Input Reference Voltage | 0.49*$V_{DDQ}$ | 0.50*$V_{DDQ}$ | 0.51*$V_{DDQ}$ | mV | 2, 3 |
| $V_{TT}$ | Termination Voltage | $V_{REF}$-0.04 | $V_{REF}$ | $V_{REF}$+0.04 | V | 4 |

Note : There is no specific device $V_{DD}$ supply voltage requirement for SSTL-1.8 compliance. However under all conditions $V_{DDQ}$ must be less than or equal to $V_{DD}$.

1. The value of $V_{REF}$ may be selected by the user to provide optimum noise margin in the system. Typically the value of $V_{REF}$ is expected to be about 0.5 x $V_{DDQ}$ of the transmitting device and $V_{REF}$ is expected to track variations in $V_{DDQ}$.
2. Peak to peak AC noise on $V_{REF}$ may not exceed +/-2% $V_{REF}$(DC).
3. $V_{TT}$ of transmitting device must track $V_{REF}$ of receiving device.
4. $V_{DDQ}$ tracks with $V_{DD}$, $V_{DDL}$ tracks with $V_{DD}$. AC parameters are measured with $V_{DD}$, $V_{DDQ}$ and $V_{DDL}$ tied together.

## Input DC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| $V_{IH}$(DC) | DC input logic high | $V_{REF}$ + 0.125 | $V_{DDQ}$ + 0.3 | V | |
| $V_{IL}$(DC) | DC input logic low | - 0.3 | $V_{REF}$ - 0.125 | V | |

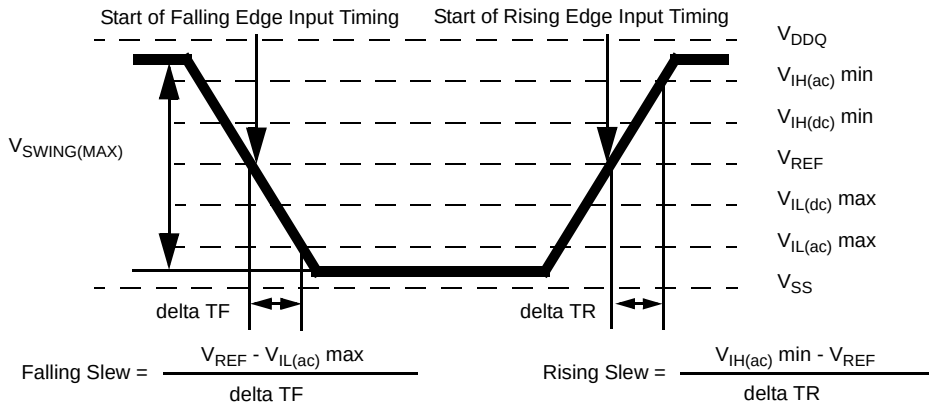
## Input AC Logic Level

| Symbol | Parameter | DDR2-400, DDR2-533 | | DDR2-667, DDR2-800 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $V_{IH}$(AC) | AC input logic high | $V_{REF}$ + 0.250 | - | $V_{REF}$ + 0.200 | | V | |
| $V_{IL}$(AC) | AC input logic low | - | $V_{REF}$ - 0.250 | | $V_{REF}$ - 0.200 | V | |

## AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|---|---|---|---|---|
| $V_{REF}$ | Input reference voltage | 0.5 * $V_{DDQ}$ | V | 1 |
| $V_{SWING(MAX)}$ | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

Notes:
1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from $V_{REF}$ to $V_{IH}$(AC) min for rising edges and the range from $V_{REF}$ to $V_{IL}$(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from $V_{IL}$(AC) to $V_{IH}$(AC) on the positive transitions and $V_{IH}$(AC) to $V_{IL}$(AC) on the negative transitions.



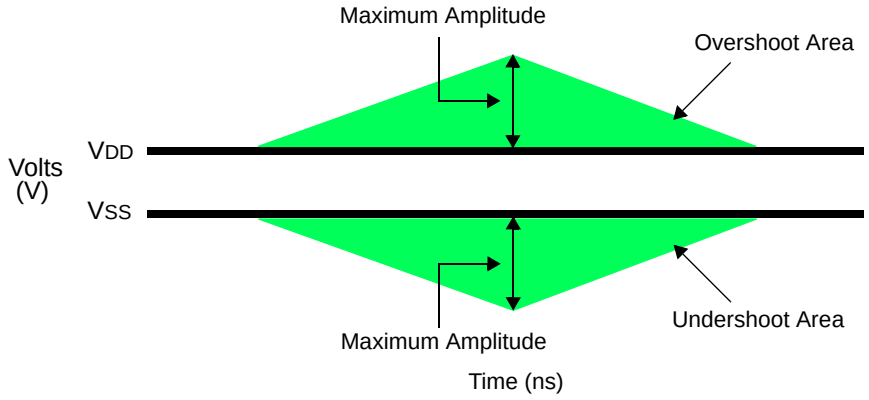

< AC Input Test Signal Waveform >

## Overshoot/Undershoot Specification

**AC Overshoot/Undershoot Specification for Address and Control Pins A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT**

| Parameter | Specification | | | |
|---|---|---|---|---|
| | DDR2-400 | DDR2-533 | DDR2-667 | DDR2-800 |
| Maximum peak amplitude allowed for overshoot area (See following figure): | 0.5(0.9)*V | 0.5(0.9)*V | 0.5(0.9)*V | 0.5(0.9)*V |
| Maximum peak amplitude allowed for undershoot area (See following figure): | 0.5(0.9)*V | 0.5(0.9)*V | 0.5(0.9)*V | 0.5(0.9)*V |
| Maximum overshoot area above VDD (See following figure). | 1.33 V-ns | 1.0 V-ns | 0.8 V-ns | 0.66 V-ns |
| Maximum undershoot area below VSS (See following figure). | 1.33 V-ns | 1.0 V-ns | 0.8 V-ns | 0.66 V-ns |

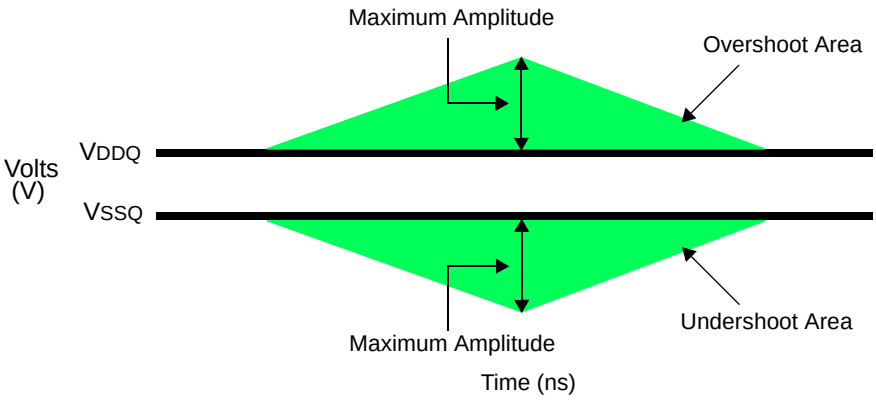
Note : The maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Register vendor datasheets will specify the maximum overshoot/undershoot induced in specific RDIMM applications. DRAM vendor datasheets will also specify the maximum overshoot/undershoot that their DRAM can tolerate. This will allow the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register will induce in the specific RDIMM application.




**AC Overshoot and Undershoot Definition for Address and Control Pins**

**AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins DQ, DQS, DM, CK, $\overline{CK}$**

| Parameter | Specification | | | |
|---|---|---|---|---|
| | DDR2-400 | DDR2-533 | DDR2-667 | DDR2-800 |
| Maximum peak amplitude allowed for overshoot area (See following figure): | 0.5V | 0.5V | 0.5V | 0.5V |
| Maximum peak amplitude allowed for undershoot area (See following figure): | 0.5V | 0.5V | 0.5V | 0.5V |
| Maximum overshoot area above VDDQ (See following figure): | 0.38 V-ns | 0.28 V-ns | 0.23 V-ns | 0.23 V-ns |
| Maximum undershoot area below VSSQ (See following figure): | 0.38 V-ns | 0.28 V-ns | 0.23 V-ns | 0.23 V-ns |




**AC Overshoot and Undershoot Definition for Clock, Data, Strobe, and Mask Pins**

Table 1. Full Strength Default Pulldown Driver Characteristics

| | Pulldown Ourrent (mA) | | | |
|---|---|---|---|---|
| Voltage (V) | Minimum(23.4 Ohms) | Nominal Default Low (18 ohms) | Nominal Default High (18 ohms) | Maximum(12.6 Ohms) |
| 0.2 | 8.5 | 11.3 | 11.8 | 15.9 |
| 0.3 | 12.1 | 16.5 | 16.8 | 23.8 |
| 0.4 | 14.7 | 21.2 | 22.1 | 31.8 |
| 0.5 | 16.4 | 25.0 | 27.6 | 39.7 |
| 0.6 | 17.8 | 28.3 | 32.4 | 47.7 |
| 0.7 | 18.6 | 30.9 | 36.9 | 55.0 |
| 0.8 | 19.0 | 33.0 | 40.9 | 62.3 |
| 0.9 | 19.3 | 34.5 | 44.6 | 69.4 |
| 1.0 | 19.7 | 35.5 | 47.7 | 75.3 |
| 1.1 | 19.9 | 36.1 | 50.4 | 80.5 |
| 1.2 | 20.0 | 36.6 | 52.6 | 84.6 |
| 1.3 | 20.1 | 36.9 | 54.2 | 87.7 |
| 1.4 | 20.2 | 37.1 | 55.9 | 90.8 |
| 1.5 | 20.3 | 37.4 | 57.1 | 92.9 |
| 1.6 | 20.4 | 37.6 | 58.4 | 94.9 |
| 1.7 | 20.6 | 37.7 | 59.6 | 97.0 |
| 1.8 | | 37.9 | 60.9 | 99.1 |
| 1.9 | | | | 101.1 |

Figure 1. DDR2 Default Pulldown Characteristics for Full Strength Driver

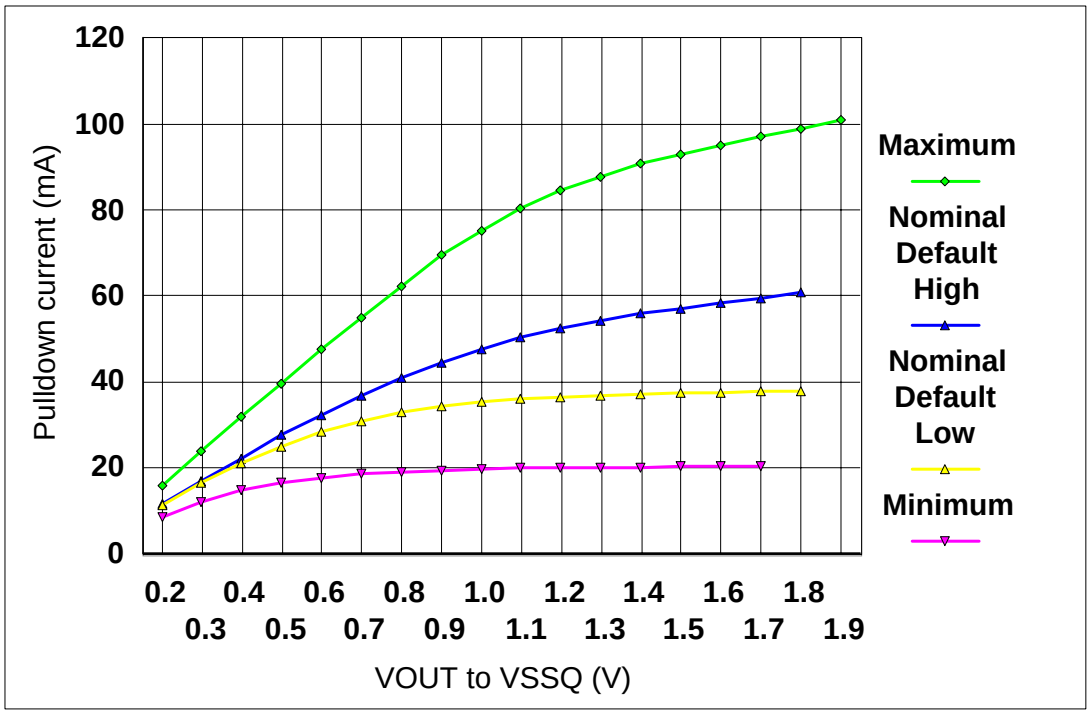


Table 2. Full Strength Default Pullup Driver Characteristics

| | Pullup Ourrent (mA) | | | |
|---|---|---|---|---|
| Voltage (V) | Minimum(23.4 Ohms) | Nominal Default Low (18 ohms) | Nominal Default High (18 ohms) | Maximum(12.6 Ohms) |
| 0.2 | -8.5 | -11.1 | -11.8 | -15.9 |
| 0.3 | -12.1 | -16.0 | -17.0 | -23.8 |
| 0.4 | -14.7 | -20.3 | -22.2 | -31.8 |
| 0.5 | -16.4 | -24.0 | -27.5 | -39.7 |
| 0.6 | -17.8 | -27.2 | -32.4 | -47.7 |
| 0.7 | -18.6 | -29.8 | -36.9 | -55.0 |
| 0.8 | -19.0 | -31.9 | -40.8 | -62.3 |
| 0.9 | -19.3 | -33.4 | -44.5 | -69.4 |
| 1.0 | -19.7 | -34.6 | -47.7 | -75.3 |
| 1.1 | -19.9 | -35.5 | -50.4 | -80.5 |
| 1.2 | -20.0 | -36.2 | -52.5 | -84.6 |
| 1.3 | -20.1 | -36.8 | -54.2 | -87.7 |
| 1.4 | -20.2 | -37.2 | -55.9 | -90.8 |
| 1.5 | -20.3 | -37.7 | -57.1 | -92.9 |
| 1.6 | -20.4 | -38.0 | -58.4 | -94.9 |
| 1.7 | -20.6 | -38.4 | -59.6 | -97.0 |
| 1.8 | | -38.6 | -60.8 | -99.1 |
| 1.9 | | | | -101.1 |

Figure 2. DDR2 Default Pullup Characteristics for Full Strength Output Driver

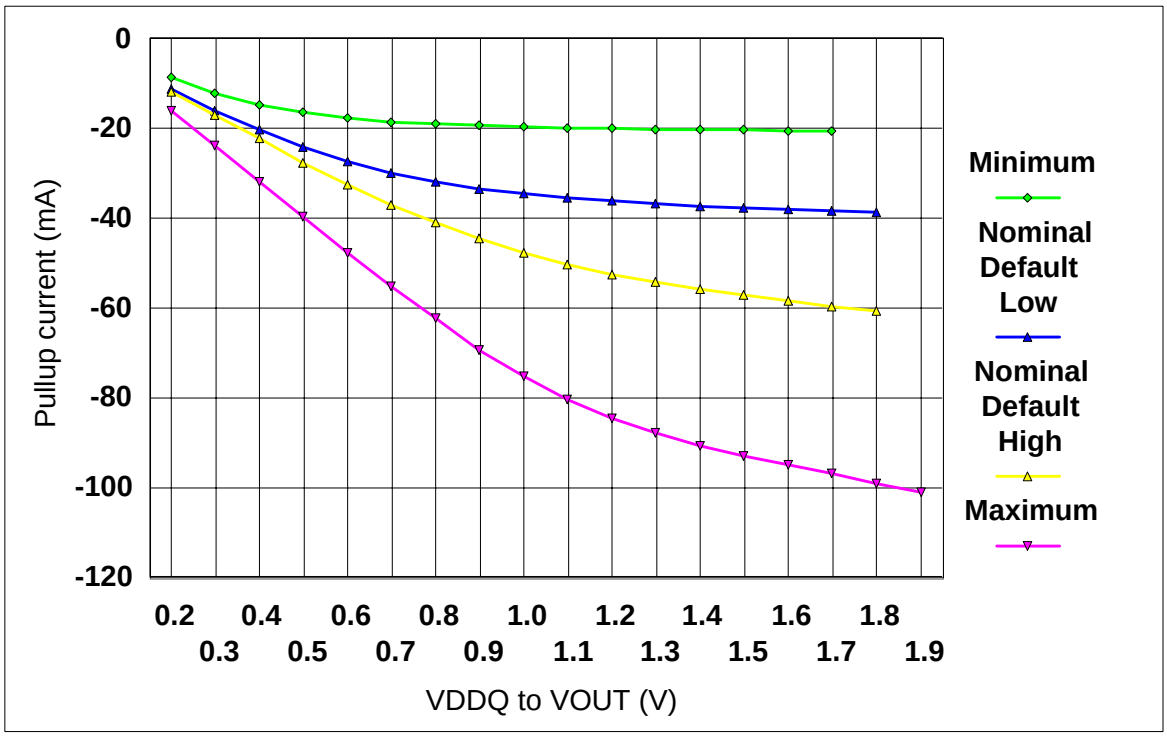


Table 3. Reduced Strength Default Pulldown Driver Characteristics

| | Pulldown Ourrent (mA) | | | |
|---|---|---|---|---|
| Voltage (V) | Minimum | Suggested IBIS Target Low | Suggested IBIS Target High | Maximum |
| 0.0 | 0.00 | 0.00 | 0.00 | 0.00 |
| 0.1 | 1.72 | 3.24 | 4.11 | 4.77 |
| 0.2 | 3.44 | 6.25 | 8.01 | 9.54 |
| 0.3 | 5.16 | 9.03 | 11.67 | 14.31 |
| 0.4 | 6.76 | 11.52 | 15.03 | 19.08 |
| 0.5 | 8.02 | 13.66 | 18.03 | 23.85 |
| 0.6 | 8.84 | 15.41 | 20.61 | 28.62 |
| 0.7 | 9.31 | 16.77 | 22.71 | 33.33 |
| 0.8 | 9.64 | 17.74 | 24.35 | 37.77 |
| 0.9 | 9.89 | 18.38 | 25.56 | 41.73 |
| 1.0 | 10.09 | 18.80 | 26.38 | 45.21 |
| 1.1 | 10.26 | 19.06 | 26.90 | 48.21 |
| 1.2 | 10.41 | 19.23 | 27.24 | 50.73 |
| 1.3 | 10.54 | 19.35 | 27.47 | 52.77 |
| 1.4 | 10.66 | 19.46 | 27.64 | 54.42 |
| 1.5 | 10.77 | 19.56 | 27.78 | 55.80 |
| 1.6 | 10.88 | 19.65 | 27.89 | 57.03 |
| 1.7 | 10.98 | 19.73 | 27.97 | 58.23 |
| 1.8 | | 19.80 | 28.02 | 59.43 |
| 1.9 | | | | 60.63 |

Figure 3. DDR2 Default Pulldown Characteristics for reduced Strength Driver

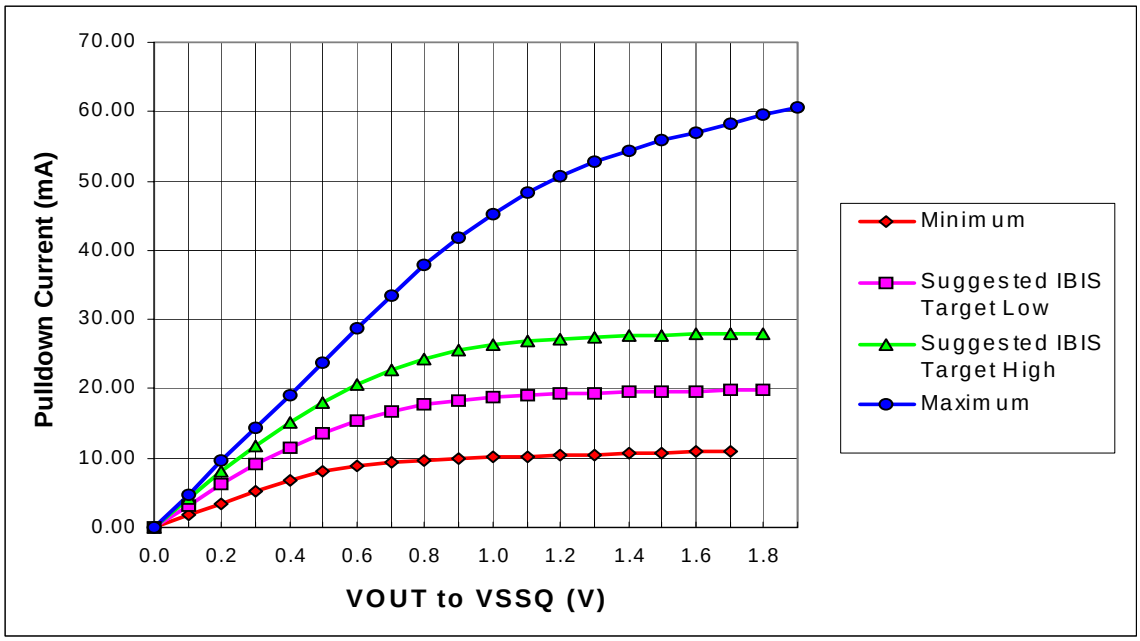
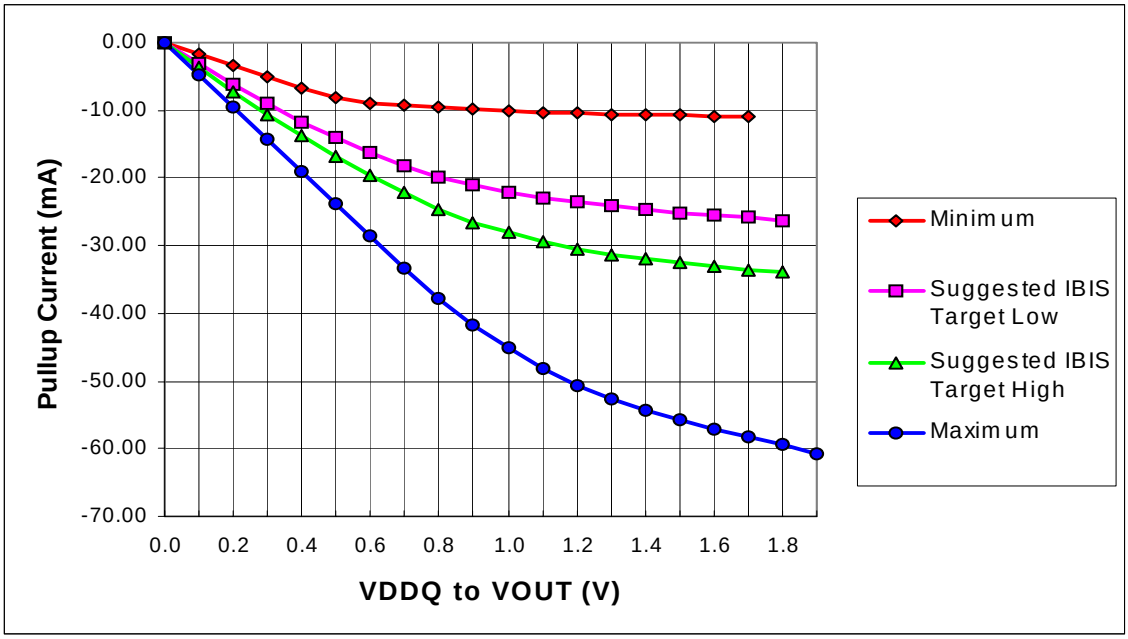


Table 4. Reduced Strength Default Pulldown Driver Characteristics

| | Pulldown Ourrent (mA) | | | |
|---|---|---|---|---|
| Voltage (V) | Minimum | Suggested IBIS Target Low | Suggested IBIS Target High | Maximum |
| 0.0 | 0.00 | -0.00 | 0.00 | 0.00 |
| 0.1 | -1.72 | -3.200 | -3.70 | -4.77 |
| 0.2 | -3.44 | -6.200 | -7.22 | -9.54 |
| 0.3 | -5.16 | -9.040 | -10.56 | -14.31 |
| 0.4 | -6.76 | -11.690 | -13.75 | -19.08 |
| 0.5 | -8.02 | -14.110 | -16.78 | -23.85 |
| 0.6 | -8.84 | -16.270 | -19.61 | -28.62 |
| 0.7 | -9.31 | -18.160 | -22.20 | -33.33 |
| 0.8 | -9.64 | -19.770 | -24.50 | -37.77 |
| 0.9 | -9.89 | -21.100 | -26.46 | -41.73 |
| 1.0 | -10.09 | -22.150 | -28.07 | -45.21 |
| 1.1 | -10.26 | -22.960 | -29.36 | -48.21 |
| 1.2 | -10.41 | -23.610 | -30.40 | -50.77 |
| 1.3 | -10.54 | -24.160 | -31.24 | -52.77 |
| 1.4 | -10.66 | -24.640 | -31.93 | -54.42 |
| 1.5 | -10.77 | -25.070 | -32.51 | -55.80 |
| 1.6 | -10.88 | -25.470 | -33.01 | -57.03 |
| 1.7 | -10.98 | -25.850 | -33.46 | -58.23 |
| 1.8 | | -26.210 | -33.89 | -59.43 |
| 1.9 | | | | -60.63 |

Figure 4. DDR2 Default Pulldown Characteristics for reduced Strength Driver



### DDR2 SDRAM Default Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS1 bits A7-A9 = '111'. Figures 1 and 2 show the driver characteristics graphically, and tables 1 and 2 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

Nominal Default 25 $^{o}$C (T case), VDDQ = 1.8 V, typical process
Minimum $T_{OPER(MAX)}$, VDDQ = 1.7 V, slow–slow process
Maximum 0 $^{o}$C (T case), VDDQ = 1.9 V, fast–fast process

### Default Output Driver Characteristic Curves Notes:

1) The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of figures 1 and 2.
2) It is recommended that the "typical" IBIS V–I curve lie within the inner bounding lines of the V–I curves of figures 1 and 2.

Table 3. Full Strength Calibrated Pulldown Driver Characteristics

| | Calibrated Pulldown Ourrent (mA) | | | | |
|---|---|---|---|---|---|
| **Voltage (V)** | **Nominal Minimum** | **Nominal Low (18.75 ohms)** | **Nominal (18 ohms)** | **Nominal (17.25 ohms)** | **Nominal Maximum (15 ohms)** |
| 0.2 | 9.5 | 10.7 | 11.5 | 11.8 | 13.3 |
| 0.3 | 14.3 | 16.0 | 16.6 | 17.4 | 20.0 |
| 0.4 | 18.7 | 21.0 | 21.6 | 23.0 | 27.0 |

Table 4. Full Strength Calibrated Pullup Driver Characteristics

| | Calibrated Pullup Ourrent (mA) | | | | |
|---|---|---|---|---|---|
| **Voltage (V)** | **Nominal Minimum (21 ohms)** | **Nominal Low (18.75 ohms)** | **Nominal (18 ohms)** | **Nominal (17.25 ohms)** | **Nominal Maximum (15 ohms)** |
| 0.2 | -9.5 | -10.7 | -11.4 | -11.8 | -13.3 |
| 0.3 | -14.3 | -16.0 | -16.5 | -17.4 | -20.0 |
| 0.4 | -18.7 | -21.0 | -21.2 | -23.0 | -27.0 |

### DDR2 SDRAM Calibrated Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in Off-Chip Driver (OCD) Impedance Adjustment. Tables 3 and 4 show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohm step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

The driver characteristics evaluation conditions are:

Nominal 25 $^{o}$C (T case), $V_{DDQ}$ = 1.8 V, typical process
Nominal Low and Nominal High 25 $^{o}$C (T case), $V_{DDQ}$ = 1.8 V, any process
Nominal Minimum $T_{OPER(MAX)}$, $V_{DDQ}$ = 1.7 V, any process
Nominal Maximum 0 $^{o}$C (T case), $V_{DDQ}$ = 1.9 V, any process